



Datasheet

IMPINJ M700 SERIES

TAG CHIP DATASHEET

IPJ-M730A-A00

IPJ-M750A-A00

OVERVIEW

Impinj® M700 series RAIN RFID tag chips provide high performance, fast inventory capability, and advanced features for next-generation, universal RAIN RFID tags. The Impinj M700 series of performance endpoint ICs, containing the Impinj M730 and M750 tag chips, can be attached to or embedded in nearly any item, globally, to enable solutions for high-speed inventory counting, loss prevention with frictionless self-checkout, and embedded tagging with seamless product returns.

The Impinj M730 IC has 128-bit EPC memory and the Impinj M750 IC has both 96-bit EPC memory and 32-bit User memory. Both Impinj ICs provide increased sensitivity, improved readability, advanced features, and are compatible with the global GS1 UHF Gen2v2 standard which ISO/IEC standardized as 18000-63.

SPECIFICATIONS SUMMARY

- Read sensitivity of up to -24 dBm with a dipole antenna
- Write sensitivity of up to -21 dBm with a dipole antenna
- 96 bits of Serialized TID with 48-bit serial number
- Two memory configuration options:
 - Impinj M730: 128 bits of EPC memory, 0 bits of User memory
 - Impinj M750: 96 bits of EPC memory, 32 bits of User memory
- Inlay compatibility between Impinj M730 and Impinj M750 tag chips
- ISO/IEC 18000-63:2015 and EPCglobal Gen2v2 compliant

FEATURES SUMMARY

- **Enhanced AutoTune™ Adaptive RF Tuning** — Optimizes performance to the tag's environment for improved readability across different materials, tag form factors, and operating frequencies
- **Enhanced Integra™ Memory Diagnostics** — Suite of diagnostics verify tag chip health and validate data encoding to consistently deliver more accurate data and reliable tags. This includes built-in memory error detection with parity checking applied throughout normal Gen2v2 operation
- **Protected Mode** enables loss prevention and protects consumer privacy by making a tag invisible to RAIN readers. The tag can be returned to normal operation and made visible to readers using a secure password
- **Short-Range Mode** decreases a tag's read range by >90% via the EPCglobal Gen2v2 *Untraceable* command.
- **Shared Access and Kill Passwords** protect tag memory blocks or permanently deactivate the tag
- **Enduro™ IC Bonding Technology** — Patented low-profile bonding pad design delivers high-quality tags for improved tag yield, reliability, durability, and optimizes eco-friendly tag performance
- **TagFocus™ Read Redundancy Prevention** — Unique algorithm prevents multiple reads of the same IC so that hard-to-read tags can be read more accurately within a complex population of tags
- **FastID™ High-Speed Reading** — Increases TID-based read speeds by 2-3x to quickly identify tags by EPC and TID
- **Monza® Self-Serialization** — Scalable built-in serialization

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1 INTRODUCTION

1.1 Scope

This datasheet defines the physical and logical specifications for Gen2-compliant Impinj M700 series tag silicon, a reader-talks-first, radio frequency identification (RFID) component operating in the UHF frequency range.

1.2 Reference Documents

The following reference documents were used to compile this datasheet:

- EPC™ Radio-Frequency Identity Protocols Generation-2 UHF RFID Protocol for Communications at 860 MHz – 960 MHz (Gen2v2 Specification, version 2.0.1 Feb 2016)
 - The conventions used in the Gen2v2 Specification (normative references, terms and definitions, symbols, abbreviated terms, and notation) were adopted in the drafting of this Impinj M730 and M750 Tag Chip Datasheet. Users of this datasheet should familiarize themselves with the Gen2v2 Specification.
- Impinj M730 and M750 Wafer Specification
- Impinj Monza Wafer Map Orientation Guide
- TID Memory Maps for Monza Self-Serialization Application Note
- EPC™ Tag Data Standards Specification 1.13
- EPCglobal “Interoperability Test System for EPC Compliant Class-1 Generation-2 UHF RFID Devices” v.2.1, Jul 2018

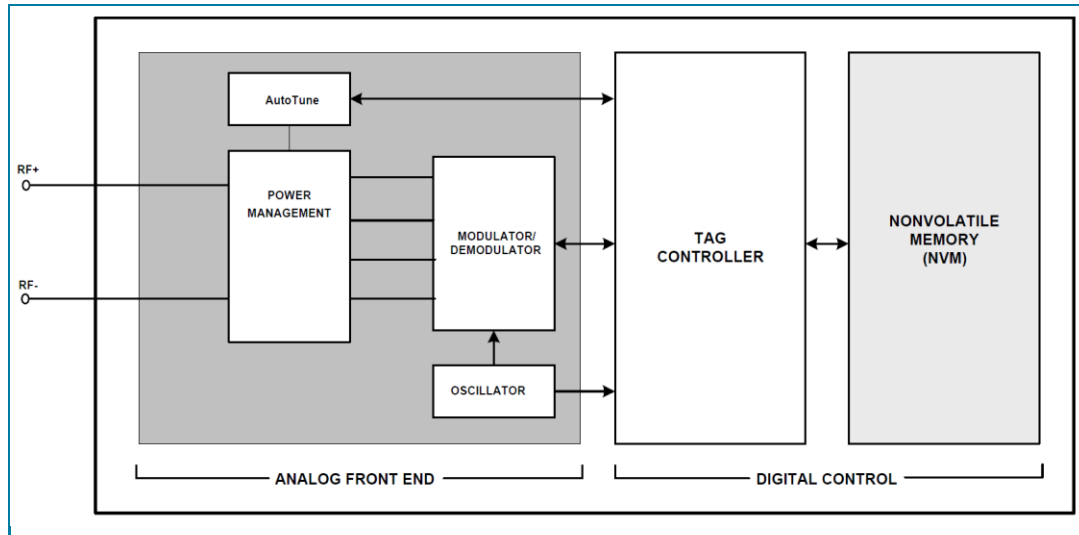
Consult these documents for more information about compliance standards and specifications.

2 FUNCTIONAL DESCRIPTION

The Impinj M700 series tag chips fully support all mandatory commands of the Gen2v2 specification as well as optional commands and features (see Support for Optional Gen2v2 Commands, section 2.2).

2.1 Impinj M700 Series Tag Chip Block Diagram

Figure 1: Block Diagram



2.1.1 Power Management

The tag is activated by proximity to an active reader. When the tag enters a reader's RF field, the Power Management block converts the induced electromagnetic field to the DC voltage that powers the chip.

2.1.2 Enhanced AutoTune

The Enhanced AutoTune block adjusts Impinj M700 series tag chip power harvesting from the inlay antenna by adjusting the chip's input capacitance. The refined tuning algorithm improves symmetry around tag resonances and widens the dynamic range of the IC sensitivity across the entire 860-960 MHz UHF spectrum. AutoTune adjustment occurs at every IC power up and is held for the remainder of the time that the tag chip is powered. For information on how to read out the AutoTune values or configure this feature, refer to AutoTune Disable and AutoTune Value, section 4.4.3.

2.1.3 Modulator/Demodulator

The Impinj M700 series tag chips demodulate any of a reader's three possible modulation formats, DSB-ASK, SSB-ASK, or PR-ASK with PIE encoding. The tag communicates to a reader via backscatter of the incident RF waveform by switching the reflection coefficient of its antenna pair between reflective and absorptive states. Backscattered data is encoded as either FM0 or Miller subcarrier modulation (with the reader commanding both the encoding choice and the data rate).

2.1.4 Tag Controller

The Tag Controller block is a finite state machine (digital logic) that carries out command sequences and performs a number of overhead duties.

2.1.5 Nonvolatile Memory

The Impinj M700 series tag chip embedded memory is nonvolatile memory (NVM) cell technology, specifically optimized for RFID applications. All programming overhead circuitry is integrated on chip. Impinj M700 series tag chip NVM provides 10,000 write cycle endurance or 10-year data retention.

The memory write speed for Impinj M700 series is 3.2 ms per *Write*, *BlockWrite*, *Lock* or *Kill* operation, for writing up to 32 bits.

The NVM block is organized into three segments:

- EPC memory:
 - Impinj M730: 128 bits
 - Impinj M750: 96 bits
 - The Protocol-Control word contains an additional 9 programmable bits
- User memory:
 - Impinj M730: 0 bits
 - Impinj M750: 32 bits
- Reserved memory, which includes the shared Access and Kill passwords, and feature and chip control words

The ROM-based Tag Identification (TID) memory contains the EPCglobal class ID, the manufacturer identification, and the model number. It also contains an extended TID consisting of a 16-bit header and 48-bit serialization.

See Table 1 for the Impinj M700 series memory organization.

Table 1: Impinj M700 Series Memory Organization

MEMORY SECTION	IMPINJ M730	IMPINJ M750
EPC	128 bits	96 bits
User	0 bits	32 bits
TID (not changeable)	Serial Number – 48 bits	Serial Number – 48 bits
	Extended TID Header – 16 bits	Extended TID Header – 16 bits
	Company/Model Number – 32 bits	Company/Model Number – 32 bits
Reserved	Chip Configuration	Chip Configuration
	Kill Password – 32 bits, shared	Kill Password – 32 bits, shared
	Access Password – 32 bits, shared	Access Password – 32 bits, shared

2.2 Support for Optional Gen2v2 Commands

Impinj M700 series tag chips support the optional commands listed in Table 2. For further details on these commands, refer to the EPC™ Radio-Frequency Identity Protocols Generation-2 UHF RFID Protocol for Communications at 860 MHz – 960 MHz (Gen2v2 Specification).

Table 2: Supported Gen2v2 Specification Commands

COMMAND	DETAILS
Access	<ul style="list-style-type: none"> • Supports full functionality of the <i>Access</i> command • Allows control of user access to write and/or lock the tag
BlockWrite	<ul style="list-style-type: none"> • Accepts valid one-word commands • Accepts valid two-word commands if pointer is an even value • Returns error code “Not supported” (00000001₂) if it receives a valid two-word command with an odd value pointer • Returns error code “Not supported” (00000001₂) if it receives a command for more than two words • Does not respond to <i>BlockWrite</i> commands of zero words
Lock	<ul style="list-style-type: none"> • Impinj M730 and M750 support the <i>Lock</i> command • Separately lockable EPC and User memory bank • Lockable access and kill password – these passwords share the same lock status and cannot be locked independently from each other. For further details on locking the shared password, see section 4.4.1.3 • The TID memory bank is perma-locked at the factory and is read only
Untraceable	<ul style="list-style-type: none"> • Impinj M730 and M750 support only the <i>Range</i> parameter of the <i>Untraceable</i> command to shift between short/reduced range and full, normal operating range. This includes supporting temporarily toggling the range. • The EPC length field (L bits) must match the EPC length field (StoredPC bits 10_n– 14_n) • For an alternative method to set a tag for short range, see section 4.4.2

Note: the Impinj M730/M750 tag chip supports all mandatory commands. However, the kill and access password have the same value and lock status.

2.3 Enhanced Integra Memory Diagnostics

Impinj M700 series tag chips have improved data integrity features that enhance encoding and data reliability. These features include Memory Parity Self-Check and the *MarginRead* command.

2.3.1 Memory Parity Self-Check

The Integra self-check feature in Impinj M700 series tag chips has been expanded to include automatic word-wise parity checking for all memory spaces. Automatic parity checking prevents tags from sending corrupt data to a reader during Gen2v2 inventory rounds or read operations.

The tag has an additional parity bit for each word stored on the chip used for implementing memory parity checks during typical Gen2v2 operations described in this section. The parity bits are used for internal parity checking and are not directly readable.

2.3.1.1 Factory Memory Parity Check

At IC power-up, parity is checked in Reserved memory words 4 - 6 and TID memory words 0 - 5. The tag will not send any response if parity fails on any of these words. If the tag backscatters an RN16, e.g. in response to a *Query* command during an inventory, the parity check has passed for this memory.

2.3.1.2 EPC Parity Check

During a typical inventory round, the EPC data, as specified by the EPC length, is checked for parity errors. If an error is detected in the EPC data at IC power-up, the tag will respond with a zero-length EPC. If an error is detected in the PC word, the tag will respond with a zero-length EPC and an inverted PacketCRC. If an error is detected in the EPC data during a normal inventory but after IC power-up, the tag will respond

with the EPC data and an inverted PacketCRC. If there are no parity errors, the tag will respond with the expected EPC data.

2.3.1.3 Read Memory Parity Check

Parity is checked on individual words of memory by issuing a *Read* command. The target word(s) will be checked for parity errors. If an error is detected, tag will respond with the read data and an inverted CRC. If there are no parity errors, the tag will respond with the expected data.

2.3.1.4 Shared Password Parity Check

Parity is checked on the shared password by issuing a *Kill* or *Access* command sequence. If an error is detected in the shared password, the tag will not be able to enter the **killed** or **secured** states and the tag will respond with the error codes shown below. If no errors are detected, the tag responds as expected and may therefore enter the **killed** or **secured** states by issuing the *Kill* or *Access* command sequences, respectively, with the correct password.

- *Kill* command sequence: tag with parity error in shared password responds with an error code as if the kill password = 0
 - Tag sends *delayed* reply with error code
- *Access* command sequence: tag with parity error in shared password responds with an error code indicating the access is disallowed
 - Tag sends error code 00000000₂

2.3.2 Recommended Memory Parity Self-Check Usage Guidelines

Memory Parity Self-Check is designed to allow reliable, automatic screening capabilities to improve quality when manufacturing RAIN RFID tags with Impinj endpoint ICs. Memory failures are rare but are a reality of RFID tag manufacturing. In RAIN RFID, there are potential points of failure throughout the tag manufacturing ecosystem before finished tags are attached to items—from the silicon manufacturing process through inlay manufacturing, label conversion, and finally the printing and encoding of finished tags. If the integrity of a tag is compromised, it should be screened out as early as possible.

The Enhanced Integra Memory Parity Self-Check provides a seamless, built-in mechanism to minimize the risk of damaged parts being put into service. Bit flips are easily screened on Impinj M700 series tag chips as they will self-report issues, checking their memory during every Gen2v2 inventory round or read operation.

- If inventory rounds or read operations complete successfully, no parity errors were detected
- If locking an Impinj M700 series tag with a non-zero password, parity will be checked on the shared password automatically during the normal lock command sequence.
 - An *Access* command is required before issuing a *Lock* command to a tag with a non-zero password
 - Parity on the shared password is checked in response to the *Access* command
 - If the *Access* command sequence is successful, no parity errors were detected in the password

2.3.3 *MarginRead* Command

MarginRead is a Gen2v2-compliant custom command supported by Impinj tag chips with Integra. This command allows a reader to explicitly verify that each bit of the tag chip NVM is strongly written and has sufficient charge margin for reliable operation. It is used for tag quality control to ensure data integrity and for failure analysis.

Table 3, Table 4, and Table 5 provide details about the custom Impinj *MarginRead* command.

Table 3: *MarginRead* Command Code

COMMAND	CODE	LENGTH	DETAILS
<i>MarginRead</i>	1110000000000001	≥ 67 bits	<ul style="list-style-type: none"> The <i>MarginRead</i> command allows checking for sufficient write margin of known data The tag must be in the open/secured state to respond to the command If a tag receives a <i>MarginRead</i> command with an invalid handle, it ignores that command The tag responds with the Insufficient Power error code if the power is too low to execute a <i>MarginRead</i> The tag responds with the Other error code if the margin is bad for a bit in the mask or if a non-matching bit is sent by the reader The <i>MarginRead</i> command is only applicable for programmable sections of the memory

Table 4: *MarginRead* Command Details

MARGINREAD COMMAND	CODE	MEM BANK	BIT POINTER	LENGTH	MASK	RN	CRC-16
#bits	16	2	EBV	8	Variable	16	16
Details	11100000 00000001	00: Reserved 01: EPC 10: TID 11: User	Starting Bit Address Pointer	Length in Bits	Mask Value	Handle	CRC-16

Table 5: *MarginRead* Command Field Descriptions

FIELD	DESCRIPTION
Mem Bank	The memory bank to access
Bit Pointer	An EBV that indicates the starting bit address of the mask
Length	Length of the mask field from 1-255 A value of zero shall result in the command being ignored
Mask	This field must match the expected values of the bits The chip checks that each bit matches what is in the mask field with margin
RN	The tag will ignore any <i>MarginRead</i> command received with an invalid handle

The tag response to the *MarginRead* Command uses the preamble specified by the TReXT value in the *Query* command that initiated the round. See Table 6 for tag response details.

Table 6: Tag Response to a Passing *MarginRead* Command

RESPONSE	HEADER	RN	CRC-16
#bits	1	16	16
Description	0	Handle	CRC-16

2.3.4 Recommended *MarginRead* Usage Guidelines

There are several ways that the *MarginRead* command could be used with Impinj M700 series tag chips. Impinj M700 series ICs are pre-serialized at the factory; the *MarginRead* command allows a programming reader to check that the pre-serialized data is written correctly and does not need to be re-encoded. Another recommended use of *MarginRead* is secondary and independent verification of the encoding quality. *MarginRead* can also be used for diagnosis when doing failure analysis on tags.

2.4 Protected Mode

The Impinj M700 series tag chips include an advanced tag data protection feature that can be used to enhance consumer privacy while supporting EAS and loss prevention capabilities.

A tag with an Impinj M700 series IC can be made invisible to RAIN RFID readers using Protected Mode. It allows a tag to become completely RF silent to all Gen2v2 commands but return to normal Gen2v2 operation when it receives the correct command sequence.

For more information on enabling Protected Mode in Impinj M700 series ICs, please request support through the Impinj Support Portal at <https://www.impinj.com/support>.

2.5 Advanced Impinj Inventory Features

Impinj tag chips support two unique, patented features designed to boost inventory performance for traditional EPC and TID-based applications:

- TagFocus mode minimizes redundant reads of strong tags, allowing the reader to focus on weak tags that are typically the last to be found. Using TagFocus, readers can suppress previously read tags by indefinitely refreshing their S1 B state.
- FastID™ mode makes TID-based applications practical by boosting TID-based inventory speeds by 2 to 3 times. Readers can inventory both the EPC and the TID without having to perform access commands. Setting the EPC word length to zero enables TID-only serialization.

2.6 Pad Descriptions

Impinj M700 series tag chips have two external Enduro pads available to the user: one RF+ pad, and one RF- pads. RF+ and RF- form a single differential antenna port, as shown in Table 7 (see also Figure 1 and Figure 2). Note that neither of these pads connects to the chip substrate.

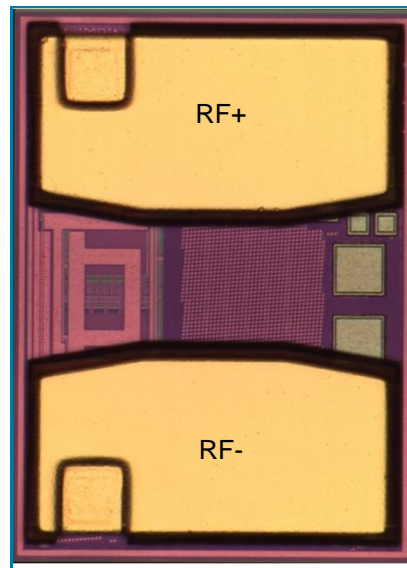
Table 7: Pad Descriptions

EXTERNAL SIGNALS	EXTERNAL PAD	DESCRIPTION
RF+	1	Differential RF Input Pads for Antenna
RF-	2	

2.7 Differential Antenna Input

All interaction with the Impinj M700 series tag chips, including generation of its internal power, air interface, negotiation sequences, and command execution, occurs via the chip's differential antenna port. The differential antenna port is connected with the RF+ pad connected to one terminal and the RF- pad connected to the other terminal.

Figure 2: Impinj M700 Series Tag Chip Die Orientation



2.8 Impinj M700 Series Antenna Reference Designs

Impinj M700 series tag chips are designed to be drop-in compatible in the same inlay antenna designs. Impinj has reference designs available for use by Impinj Endpoint IC customers under the terms of the Impinj Antenna License Agreement.

Access to these reference design documents is restricted. To access these documents, users must obtain access permission by creating an Impinj access account and submitting a request form through the Impinj Partner Access page¹. Once Impinj has accepted their request, users can use their access credentials to view the Impinj Endpoint IC reference design documents page on the Support Portal².

2.9 Impinj M700 Series Tag Chip Dimensions

Chip dimensions:

- 396.7 μm x 286.7 μm rectangular die size
- 126.9 μm x 254.7 μm pad size
- 111 μm pad spacing at center of die
- 137.3 μm pad spacing at edge of die

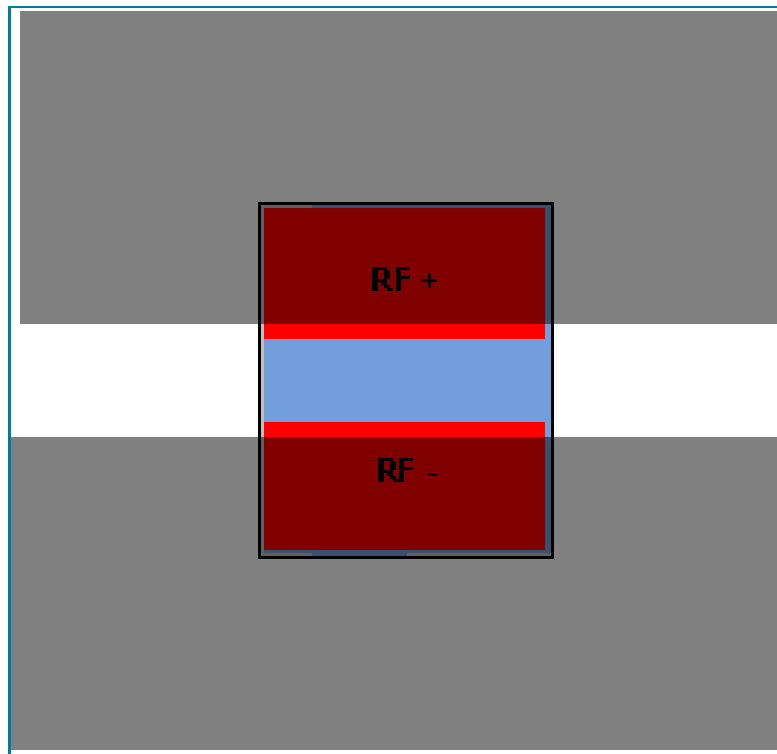
3 INTERFACE CHARACTERISTICS

This section describes the RF interface of the tag chip and the modulation characteristics of both communication links: reader-to-tag (Forward Link) and tag-to-reader (Reverse Link).

3.1 Antenna Connections

Figure 3 shows antenna connections for Impinj M700 series tag chips.

Figure 3: Antenna Connection for Inlay Production



This connection configuration for inlay production connects the Impinj M700 series tag chip RF+ pad to one antenna terminal and the RF- pad to the opposite polarity terminal. Enduro pads allow relatively coarse antenna geometry, and thus enable relaxed resolution requirements for antenna patterning compared to bumped products. The diagram in Figure 3 shows the recommended antenna trace arrangement and chip placement, with antenna traces partially overlapping the Enduro pads but not extending into the clear space between Enduro pads.

3.2 Impedance Parameters

To realize the full performance potential of the Impinj M700 series tag chips, it is imperative that the antenna present the appropriate impedance at its terminals. A simplified lumped element tag chip model, shown in Figure 4, is the conjugate of the optimum source impedance, which is *not* equal to the chip input impedance. This indirect, source-pull method of deriving the port model is necessary due to the non-linear, time-varying nature of the tag RF circuits. The model is a good mathematical fit for the chip over a broad frequency range.

The lumped element values are listed in Table 8, where C_{mount} is the parasitic capacitance due to the antenna trace overlap with the chip surface, C_p appears at the chip terminals and is intrinsic to the chip, and R_p represents the energy conversion and energy absorption of the RF circuits.

Figure 4: Tag Chip Linearized RF Model

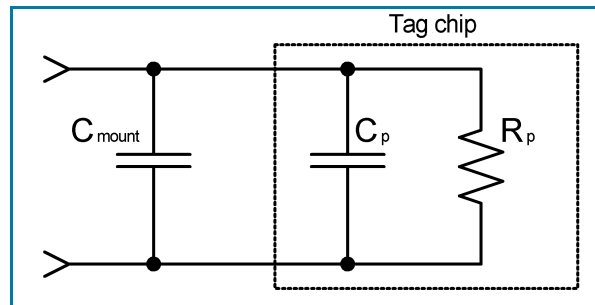


Table 8 shows the values for the chip port model for Impinj M700 series tag chips, which apply to all frequencies of the primary regions of operation (including North America and Europe).

Table 8: Impinj M700 Series RF Parameters

PARAMETER	TYPICAL VALUE	COMMENTS
R_p	2.37 kOhm	Calculated for linearized RF model shown in Figure 4.
C_p	0.93 pF	Intrinsic chip capacitance when AutoTune is mid-range, including Enduro pads.
C_{mount}	0.09 pF	Typical capacitance due to adhesive and antenna mount parasitics.
Total Load Capacitance	1.02 pF	Total load capacitance presented to antenna model of Figure 4 is: $C_p + C_{\text{mount}}$
Read Sensitivity	- 24.0 dBm	Measured in a 50-ohm system using a response to a <i>Query</i> command with a +2.15 dBi gain ideal dipole antenna.
Write Sensitivity	- 21.0 dBm	

3.3 Reader-to-Tag (Forward Link) Signal Characteristics

Table 9: Forward Link Signal Parameters

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	COMMENTS
RF Characteristics					
Carrier Frequency	860		960	MHz	North America: 902–928 MHz Europe: 865–868 MHz
Maximum RF Field Strength			+20	dBm	Received by a tag with dipole antenna while sitting on a maximum power reader antenna
Modulation		DSB-ASK, SSB-ASK, or PR-ASK			Double and single sideband amplitude shift keying; phase-reversal amplitude shift keying
Data Encoding		PIE			Pulse-interval encoding
Modulation Depth	80		100	%	(A-B)/A, A=envelope max., B=envelope min.
Ripple, Peak-to-Peak			5	%	Portion of A-B
Rise Time ($t_{r,10-90\%}$)	0		0.33Tari	sec	
Fall Time ($t_{f,10-90\%}$)	0		0.33Tari	sec	
Tari*	6.25		25	μ s	Data 0 symbol period
PIE Symbol Ratio	1.5:1		2:1		Data 1 symbol duration relative to Data 0
Duty Cycle	48		82.3	%	Ratio of data symbol high time to total symbol time
Pulse Width	MAX(0.26 5Tari,2)		0.525Tari	μ s	Pulse width defined as the low modulation time (50% amplitude)

*Values are nominal minimum and nominal maximum, and do not include frequency tolerance. Apply appropriate frequency tolerance to derive absolute periods and frequencies.

3.4 Tag-to-Reader (Reverse Link) Signal Characteristics

Table 10: Reverse Link Signal Parameters

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	COMMENTS
Modulation Characteristics					
Modulation		ASK			FET Modulator
Data Encoding		Baseband FM0 or Miller Subcarrier			
Change in Modulator Reflection Coefficient $ \Delta\Gamma $ due to Modulation		0.8			$ \Delta\Gamma = \Gamma_{reflect} - \Gamma_{absorb} $ (per read/write sensitivity, Table 8)
Duty Cycle	45	50	55	%	
Symbol Period ¹	1.5625		25	μs	Baseband FM0
	3.125		200	μs	Miller-modulated subcarrier
Miller Subcarrier Frequency*	40		640	kHz	

* Values are nominal minimum and nominal maximum, and do not include frequency tolerance. Apply appropriate frequency tolerance to derive absolute periods and frequencies.

4 TAG MEMORY

4.1 Impinj M730 Tag Chip Memory Map

Table 11: Impinj M730 Physical/Logical Memory Map

MEMORY BANK NUMBER	MEMORY BANK NAME	MEMORY BANK BIT ADDRESS	BIT ADDRESS															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
10 ₂	TID (ROM)	80 _h -8F _h	S0	S2	S3	S0	SL	S2	SL	S3	RFU[7:0] = 00 _h							
		50 _h -5F _h	TID_Serial[15:0]															
		40 _h -4F _h	TID_Serial[31:16]															
		30 _h -3F _h	TID_Serial[47:32]															
		20 _h -2F _h	Extended TID Header = 2000 _h															
		10 _h -1F _h	MDID[3:0] = 1 _h				Model Number = 191 _h											
		00 _h -0F _h	1	1	1	0	0	0	1	0	1	0	0	MDID[8:4] = 00 _h				
01 ₂	EPC (NVM)	90 _h -9F _h	EPC[15:0]															
		80 _h -8F _h	EPC[31:16]															
		70 _h -7F _h	EPC[47:32]															
		60 _h -6F _h	EPC[63:48]															
		50 _h -5F _h	EPC[79:64]															
		40 _h -4F _h	EPC[95:80]															
		30 _h -3F _h	EPC[111:96]															
		20 _h -2F _h	EPC[127:112]															
		10 _h -1F _h	Protocol-Control Bits (PC)															
		00 _h -0F _h	CRC-16															
00 ₂	RESERVED (NVM)	140 _h -14F _h	RFU[12:0]=000 _h												ATV[2:0]			
		70 _h -7F _h	Factory Calibration C[15:0]															
		60 _h -6F _h	Factory Calibration B[15:0]															
		50 _h -5F _h	Factory Calibration A[15:0]															
		40 _h -4F _h	Internal Configuration[15:5]										SR	Internal Configuration[3:1]		A		
		30 _h -3F _h	Shared Access Password[15:0]															
		20 _h -2F _h	Shared Access Password[31:16]															
		10 _h -1F _h	Shared Kill Password[15:0]															
		00 _h -0F _h	Shared Kill Password[31:16]															

Note: The Impinj M730 and M750 tag chips have a single 32-bit password; the Access and Kill passwords are shared and aliased over one another.

4.2 Impinj M750 Tag Chip Memory Map

Table 12: Impinj M750 Physical/Logical Memory Map

MEMORY BANK NUMBER	MEMORY BANK NAME	MEMORY BANK BIT ADDRESS	BIT ADDRESS															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
11 ₂	USER (NVM)	10 _h -1F _h	User[15:0]															
		00 _h -0F _h	User[31:16]															
10 ₂	TID (ROM)	80 _h -8F _h	S0	S2	S3	S0	SL	S2	SL	S3	RFU[7:0] = 00 _h							
		50 _h -5F _h	TID_Serial[15:0]															
		40 _h -4F _h	TID_Serial[31:16]															
		30 _h -3F _h	TID_Serial[47:32]															
		20 _h -2F _h	Extended TID Header = 2000 _h															
		10 _h -1F _h	MDID[3:0] = 1 _h				Model Number = 190 _h											
		00 _h -0F _h	1	1	1	0	0	0	1	0	1	0	0	MDID[8:4] = 00 _h				
01 ₂	EPC (NVM)	70 _h -7F _h	EPC[15:0]															
		60 _h -6F _h	EPC[31:16]															
		50 _h -5F _h	EPC[47:32]															
		40 _h -4F _h	EPC[63:48]															
		30 _h -3F _h	EPC[79:64]															
		20 _h -2F _h	EPC[95:80]															
		10 _h -1F _h	Protocol-Control Bits (PC)															
		00 _h -0F _h	CRC-16															
00 ₂	RESERVED (NVM)	140 _h -14F _h	RFU[12:0]=000 _h													ATV[2:0]		
		70 _h -7F _h	Factory Calibration C[15:0]															
		60 _h -6F _h	Factory Calibration B[15:0]															
		50 _h -5F _h	Factory Calibration A[15:0]															
		40 _h -4F _h	Internal Configuration[15:5]										SR	Internal Configuration[3:1]			A	
		30 _h -3F _h	Shared Access Password[15:0]															
		20 _h -2F _h	Shared Access Password[31:16]															
		10 _h -1F _h	Shared Kill Password[15:0]															
		00 _h -0F _h	Shared Kill Password[31:16]															

Note: The Impinj M730 and M750 tag chips have a single 32-bit password; the Access and Kill passwords are shared and aliased over one another.

4.3 Logical vs. Physical Bit Identification

For the purposes of distinguishing most significant from least significant bits, a logical representation is used in this datasheet where MSBs correspond to large bit numbers and LSBs to small bit numbers. For example, Bit 15 is the logical MSB of a memory row in the memory map. Bit 0 is the LSB. A multi-bit word represented by WORD[N:0] is interpreted as MSB first when read from left to right. This convention should not be confused with the physical bit address indicated by the rows and column addresses in the memory map; the physical bit address, used for the memory bank bit addresses, describes the addressing used to access the memory.

4.4 Reserved Memory

Reserved memory contains the Access and Kill passwords, which are programmed to zero. It also contains two user configuration bits, which may only be changed in the **secured** state with a non-zero access password unless otherwise noted. The tag will transition from the **open** to **secured** state by receiving an Access command with correct access password.

- SR = the short range bit. This bit is set to zero at the factory. When this bit set to one, the chip will operate in a short range mode. The chip will not respond at all unless it is in short range. This bit may be changed from the **secured** state with a non-zero password
- A = the AutoTune disable bit. This bit is set to zero at the factory. When the AutoTune disable bit is zero AutoTune works as normal. When the bit is one, AutoTune is disabled and the capacitance on the front end assumes the mid-range value. This bit may be changed from the **secured** state with a zero or non-zero password.

To write these two bits a *Write* command or single word *BlockWrite* command must be issued to word 4 of Reserved memory. These bits must be written at the same time. These bits may be changed multiple times. When writing to this word to set the configuration bits, use the payloads as shown in Table 13. The AutoTune value is marked ATV[2:0] in word 14_h. The AutoTune value represents the tuning capacitance scale, from zero to four.

Table 13: Writing User Configurable Bits, Word 4_h of Reserved Memory

PAYLOAD (HEX)	PAYLOAD (BINARY)	SHORT RANGE BIT, SR	AUTOTUNE DISABLE BIT, A	COMMENTS
0000	0000 0000 0000 0000	0	0	Default values. Tag will be in normal range and AutoTune is enabled.
0010	0000 0000 0001 0000	1	0	Tag will be in short range with AutoTune enabled.
0001	0000 0000 0000 0001	0	1	Tag will be in normal range with AutoTune disabled.
0011	0000 0000 0001 0001	1	1	Tag will be in short range with AutoTune disabled.

*Note: This word must be written to in the **secured** state. If changing the SR bit, the tag must also have a non-zero access password, entering the **secured** state using the Access command.*

4.4.1 Shared Access and Kill Password

Impinj M700 series tag chips have a single 32-bit password; the access and kill passwords are shared and aliased over one another. The same password is used for both *Access* and *Kill* commands. *Write*, *BlockWrite* or *Lock* commands to the access password will affect the kill password and vice versa. The password may be read or written from either address. Multi-row reads of the Reserved memory bank will return the same password for words 0-1 and 2-3. The default value for the shared password is all zeroes.

Impinj M700 series tag chips will respond to *Access*, *Kill* and *Lock* commands as if the access and kill passwords were logically independent even though they share the same physical memory.

4.4.1.1 Access Password

The single shared 32-bit password functions as the access password in Reserved memory 20_h to 3F_h, MSB first. The default value is all zeroes. Tags with a non-zero access password will require a reader to issue this password as part of an *Access* command before transitioning to the **secured** state. The password stored in the access password location will always have the same value and lock status as the kill password.

4.4.1.2 Kill Password

The single shared 32-bit password functions as the kill password in Reserve Memory 00_h to 1F_h, MSB first. The default value is all zeroes. Tags with a non-zero kill password will require a reader to issue this password as part of *Kill* command before permanently transitioning to the **killed** state. Tags in the **killed** state will not respond to any commands. A tag will not execute a kill operation if its kill password is all zeroes.

4.4.1.3 Locking Password

Impinj M700 series tag chips must have the access and kill passwords locked in the same way. The table below lists specific examples of valid payloads for locking the *Access* and *Kill* passwords. It is possible to lock additional memory alongside the passwords as well – additional payloads are supported as long as the access and kill password lock settings do not conflict. If the payload for the *Lock* command is not valid, the tag chip will respond back with an error code “Not supported” (00000001_b). For further details about the *Lock* command, refer to the Gen2v2 specification.

Table 14: Supported *Lock* Command Payloads for Locking Passwords

LOCK COMMAND PAYLOAD (HEX)	LOCK COMMAND PAYLOAD (BINARY)	DESCRIPTION
A0000	1010 0000 0000 0000 0000	Access and kill passwords are unlocked and are readable or writable from the open or secured states.
F0000	1111 0000 0000 0000 0000	Access and kill passwords are permanently unlocked and are readable or writable from the open or secured states.
A0280	1010 0000 0010 1000 0000	Access and kill passwords are locked and are readable or writable from the secured state but not from the open state.
F03C0	1111 0000 0011 1100 0000	Access and kill passwords are permanently locked and are not readable or writable from any.

Note: The *Lock* command must be issued to a tag in the **secured** state. There are additional valid configuration options not listed above.

4.4.2 Short Range Mode

Impinj M700 series tag chips come with a short-range capability to enhance consumer privacy. The short range bit (SR) in Reserved memory may be written when the tag is in the **secured** state with a non-zero access password. The tag chip would require an *Access* command with the correct access password to transition from the **open** to **secured** state.

- The factory programmed value of the short range bit is zero, which means the tag operates at full range and short range is disabled.
- To enable short range, a reader writes the SR bit to a one. The tag will only respond when it is near the reader, reducing the IC’s read range to less than 1/10 of its normal range.
- To disable short range mode, a reader writes the SR bit to a zero.

Refer to Table 13 for example values to configure bits in Reserved memory.

Short range may also be configured using the Gen2v2 *Untraceable* command by specifying the *range* field as described below. The tag must be in the **secured** state with a non-zero access password in order to use the *Untraceable* command.

- If the *range* field is set to 10₂: the SR bit will be set to one and the tag will be set to short range operation.
- If the *range* field is set to 00₂: the SR bit will be set to zero and the tag will be set to normal range operation.
- If the *range* field is set to 01₂: the SR bit will not be changed but the tag will operate as per the inverse of the SR bit value. For example:
 - If the tag is in short range with SR = 1, and in the **secured** state when it receives an *Untraceable* command with range = 01₂, it will function in normal range operation until it loses energy. This may be used to ensure that a reader has enough power to talk to a short range tag before committing the change to memory.

4.4.3 AutoTune Disable and AutoTune Value

The AutoTune disable bit is in word 04_h, marked A in the memory map. The AutoTune value is marked ATV[2:0] in word 14_h. The AutoTune value represents the tuning capacitance scale, from zero to four. A value of zero removes 100 fF of capacitance across the RF input of the tag and a value of four adds 100 fF across the RF input of the chip. See Table 15 for the mapping between AutoTune value and the change in input capacitance. A reader acquires the AutoTune value by issuing a single word *Read* command to word 14_h in the Reserved memory bank. The AutoTune value is not writable.

- The factory programmed value of the AutoTune disable bit is zero, enabling AutoTune by default.
- To disable AutoTune, a reader writes the A bit to a one. When the AutoTune bit is disabled, the capacitance across the RF input is set to 0 fF. Note that the readout of AutoTune value represents the value the IC would have tuned to with AutoTune enabled, and not the current capacitance across the RF input to the tag.
- To re-enable AutoTune, a reader writes the A bit to a zero.

Refer to Table 13 for example values to configure bits in Reserved memory.

Table 15: AutoTune Value

AUTOTUNE VALUE	CHANGE IN INPUT CAPACITANCE (FF)
0h	-100
1h	-40
2h	0
3h	+40
4h	+100

4.5 EPC Memory (EPC Data, Protocol Control Bits, and CRC16)

As per the Gen2v2 specification, tag chip EPC memory contains a 16-bit cyclic-redundancy check word (CRC16) at memory addresses 00_h to 0F_h; the 16 protocol-control bits (PC) at memory addresses 10_h to 1F_h; and an EPC value beginning at address 20_h.

4.5.1 CRC16

The tag calculates the CRC16 upon power-up over the stored PC bits and the EPC specified by the EPC length field in the stored PC.

4.5.2 Protocol Control Bits

The 16 protocol control bits, or PC word, include a five-bit EPC length, a one-bit read-only User memory indicator (UMI), a one-bit read-only extended protocol control indicator (XI), and nine bits of programmable memory from 17_h to 1F_h for the numbering system identifier toggle bit, T, and either Reserved for Future Use or Application Family Identifier (RFU or AFI), bits 18_h to 1F_h.

- For Impinj M730 tag chips, the UMI bit is set to 0 to indicate the absence of User memory. The factory default PC word value is 3000_h.
- For Impinj M750 tag chips, the UMI bit is set to 1 to indicate the presence of User memory. The factory default PC word value is 3400_h.

For more details about the PC field or the CRC16, see the Gen2v2 specification.

4.5.3 EPC Data

The EPC memory bank of Impinj M730 and M750 tag chips supports a maximum EPC size of 128 bits and 96 bits respectively (see Table 1). The default configuration from the factory, however, is for a 96-bit EPC. It is possible to adjust the EPC length according to the parameters laid out in the Gen2v2 standard by adjusting the five-bit EPC length in the PC word. The EPC value written into the chip from the factory is listed below in Table 16. The “X” nibbles in the pre-programmed EPC are pre-serialized values that follow the Impinj Monza Self-Serialization formula for Impinj M700 series tag chips.

For more details on the pre-serialization formula used to generate the factory-programmed EPC, refer to the TID Memory Maps for Monza Self-Serialization³.

Table 16: EPC at Factory-Program

IMPINJ PART NUMBER	TAG CHIP MODEL	FACTORY DEFAULT PC BITS (HEX)	EPC VALUE PRE-PROGRAMMED AT THE FACTORY (HEX)
IPJ-M730A-A00	Impinj M730	3000	E280 1191 A5XX XXXX XXXX XXXX
IPJ-M750A-A00	Impinj M750	3400	E280 1190 A5XX XXXX XXXX XXXX

4.6 Tag Identification (TID) Memory

The ROM-based Tag Identification memory contains Impinj-specific data as shown in Table 17.

- The GS1-assigned 9-bit Manufacturer Identifier (MDID) for Impinj is 000000001₂ and is located in TID memory bit locations 0B_h-13_h. (Note: the location of the MDID is shown in Tag Memory, section 4, and the bit details are given in Table 17.)
- Bit 08_h is the XTID indicator bit; X has a value of 1 to indicate the presence of an extended TID, consisting of a 16-bit header and a 48-bit serialization. The Impinj M730/M750 tag chip model number is located in TID memory bits locations 14_h-1F_h. The EPCglobal™ Class ID (E2_h) is stored in TID bit locations 00_h-07_h.
- TID bit locations 80_h-87_h contain read-only flag state bits. The flag state values are mapped to memory and may be used to read the current flag states or may be used for tag filtering with the *Select* command. For the S0, S2 and S3 bits, a value of 0 indicates the tag is in the A state for the given session, and a value of 1 indicates the tag is in the B state. If the SL flag is asserted, the SL bit will be 1; if de-asserted, the SL bit will be 0.

Using any combination of these bits allows for selected tags based on any or all of these states through a single *Select* command.

Table 17: TID Memory Details

MEMORY BANK NUMBER	MEMORY BANK NAME	MEMORY BANK BIT ADDRESS	BIT ADDRESS																
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
10 ₂	TID (ROM)	80 _h -8F _h	S0	S2	S3	S0	SL	S2	SL	S3	RFU[7:0] = 00 _h								
		50 _h -5F _h	TID_SERIAL[15:0]																
		40 _h -4F _h	TID_SERIAL[31:16]																
		30 _h -3F _h	TID_SERIAL[47:32]																
		20 _h -2F _h	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		10 _h -1F _h	MDID[3:0]				<i>Impinj M730/M750 Model Number</i>												
			0	0	0	1	0	0	0	1	1	0	0	1	0	0	0	0	X ¹
00 _h -0F _h	EPCglobal™ Class ID								X	MDID[8:4]									
	1	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0		

¹X = 1 for *Impinj M730* and X=0 for *Impinj M750*

4.7 User Memory

The *Impinj M750* tag chip User memory bank contains 32 bits of memory: two 16-bit words at memory addresses 00_h to 1F_h. The *Impinj M730* tag chip contains no User memory bank. For further details about writing to User memory, refer to the Gen2v2 specification.

5 ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed in this section may cause permanent damage to the tag chip. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this datasheet is not guaranteed or implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.1 Temperature

The tag chip is designed to be used within the temperature ranges listed in Table 18. These ranges specify the operating, storage and survival conditions for the tag chip. Tag functional and performance requirements are met over the operating range, unless otherwise specified.

Table 18: Temperature Parameters

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	COMMENTS
Extended Operating Temperature	-40		+85	°C	Default range for all functional and performance requirements except write operations. Write operations are limited to the Gen2 extended temperature range maximum of 65°C.
Storage Temperature	-40		+85/125	°C	At 125°C data retention is 1 year
Assembly Survival Temperature			+260	°C	Applied for one minute
Temperature Rate of Change			4	°C / sec	During operation

5.2 Electrostatic Discharge (ESD) Tolerance

The tag chip is guaranteed to survive ESD as specified in Table 19.

Table 19: ESD Limits

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	COMMENTS
ESD			2,000	V	HBM (Human Body Model)

5.3 NVM Use Model

Tag memory is designed to endure 10,000 write cycles or retain data for 10 years.

6 ORDERING INFORMATION

Contact sales@impinj.com for ordering support.

Table 20: Ordering Information

PART NUMBER	FORM	PRODUCT	PROCESSING FLOW
IPJ-M730A-A00	Wafer	Impinj M730 tag chip	Padded, thinned (to ~120 μm) and diced
IPJ-M750A-A00	Wafer	Impinj M750 tag chip	Padded, thinned (to ~120 μm) and diced

7 EXTERNAL REFERENCES

¹ Support Link: *Impinj Restricted Access Request Form* (<https://access.impinj.com/prtlaccessrequest>)

² Support Link: *Monza Reference Design Documents & Downloads* (<https://support.impinj.com/hc/en-us/sections/200454558-Monza-Reference-Design-Documents-Downloads>) – Note: These documents are restricted and require access permission from Impinj.

³ Support Link: *TID Memory Maps for Monza Self-Serialization* (<https://support.impinj.com/hc/en-us/articles/203444983-TID-Memory-Maps-for-Monza-Self-Serialization>)

8 NOTICES

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