Application Note

IMPINJ M700 SERIES AND M800 SERIES TAG CHIPS

ENCODING RECOMMENDATIONS

Version 1.0

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1 INTRODUCTION

The Impinj M700 series and M800 series RAIN RFID tag chips provide high performance, fast inventory capability, and advanced features for next-generation, universal RAIN RFID tags. This document highlights important information and outlines general guidance for encoding Impinj M700 series and M800 series tag chips.

For additional information about these tag chips, please refer to the Impinj M700 series and M800 series Datasheets on the Impinj Support Portal at https://www.impinj.com/support.

Users may use this document alongside the whitepaper "Ensuring Encoding Quality - Service Bureau Best Practices for Monza Chips," also available through the Impinj Support Portal.

2 ENCODING CONSIDERATIONS

2.1 Encoding Overview

Note the following details when encoding Impinj M700 series and M800 series tag chips:

- The kill and access passwords are always the same value and have the same lock status
- Impinj M770 and M775 tags can be put into Unkillable mode by encoding the UK bit in Reserved memory, as detailed in section 2.2.3.1. This requires the tag to be in the secured state with a non-zero access password. The Impinj M700 & M800 series Datasheets cover these methods in more detail.
- The memory map of Impinj M800 series tags is selectable by encoding the M bit in Reserved memory, as detailed in section 2.2.3.2. This bit may be written only once from the secured state with a zero or non-zero password.
- The memory write speed for Impinj M700 series is 3.2 ms per *Write*, *BlockWrite*, *Lock, Kill*, or *Untraceable* operation, for writing up to 32 bits. The memory write speed for Impinj M800 series is 2.9 ms per *Write*, *BlockWrite*, *Lock, Kill*, or *Untraceable* operation, for writing up to 32 bits.

2.2 Tag Chip Memory Overview

The primary difference between the Impinj M730 and M830 tag chips, as compared with other M700 series and M800 series chips, is the presence of tag chip user memory. Each chip may be identified by the tag model number in the TID memory. Table 1 summarizes the memory configuration and the TID identification.

Table 1: Impinj M700 Series and M800 Series Memory Organization

PRODUCT	FIRST 32 BITS OF TID (HEX)	FACTORY DEFAULT PC WORD (HEX)	EPC MEMORY SIZE (BITS)	USER MEMORY SIZE (BITS)	SHARED ACCESS/KILL PWD
Impinj M730	E280 1191	3000	128	0	Yes
Impinj M750	E280 1190	3400	96	32	Yes
Impinj M770	E280 11A0	3400	128	32	Yes
Impinj M775	E2C0 11A2	3400	128	32	Yes
Impinj M780	E280 11C0	3400	496	128	Yes
Impinj M781	E280 11C1	3400	128	512	Yes
Impinj M830	E280 11B0	3000	128	0	Yes
Impinj M850	E280 11B0	3400	96	32	Yes

Table 2: Impinj M770 and M775 Reserved Memory Map

MEMORY BANK NUMBER	MEMORY BANK NAME	MEMORY BANK BIT ADDRESS	BIT ADDRESS															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00_2	RESERVED (NVM)	140_h-$14F_h$	RFU[12:0]=000_h													ATV[2:0]		
		70_h-$7F_h$	Factory Calibration C[15:0]															
		60_h-$6F_h$	Factory Calibration B[15:0]															
		50_h-$5F_h$	Factory Calibration A[15:0]															
		40_h-$4F_h$	Configuration[15:4]												UK	Configuration[2:0]		
		30_h-$3F_h$	Shared Access Password[15:0]															
		20_h-$2F_h$	Shared Access Password[31:16]															
		10_h-$1F_h$	Shared Kill Password[15:0]															
		00_h-$0F_h$	Shared Kill Password[31:16]															

Table 3: Impinj M830 and M850 Reserved Memory Map

MEMORY BANK NUMBER	MEMORY BANK NAME	MEMORY BANK BIT ADDRESS	BIT ADDRESS															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00_2	RESERVED (NVM)	140_h-$14F_h$	RFU[12:0]=000_h													ATV[2:0]		
		70_h-$7F_h$	Factory Calibration C[15:0]															
		60_h-$6F_h$	Factory Calibration B[15:0]															
		50_h-$5F_h$	Factory Calibration A[15:0]															
		40_h-$4F_h$	Configuration[15:4]												M	Configuration[2:0]		
		30_h-$3F_h$	Shared Access Password[15:0]															
		20_h-$2F_h$	Shared Access Password[31:16]															
		10_h-$1F_h$	Shared Kill Password[15:0]															
		00_h-$0F_h$	Shared Kill Password[31:16]															

Note: The Impinj M700 series and M800 series tag chips have a single 32-bit password; the Access and Kill passwords are shared and aliased over one another.

2.2.1 Encoding the Shared Password

For encoding the shared password to the tag, Impinj recommends encoding the access password only at Reserved memory words 2-3. This will set the kill password to the same value automatically.

2.2.2 Locking Tag Memory

Impinj M700 series and M800 series tag chips must have the access and kill passwords locked in the same way. The table below lists specific examples of valid payloads for locking the *Access* and *Kill* passwords. Users can lock additional memory along with passwords as well. The tag chip supports additional payloads unless the access and kill password lock settings conflict. If the payload for the *Lock* command is not valid,

the tag chip will respond back with an error code “Not supported” (00000001_b). For example, if the user issues a payload to lock or permalock User memory for an Impinj M730 or M830 tag, which has no User memory, the tag will respond with the error code “Not supported” (00000001_b) if it is in the secured state and receives a *Lock* command with such a payload.

Locking the access/kill passwords make the passwords read/write protected. Locking EPC or User memory makes it password write protected. Permalocking the access/kill passwords will make them permanently read/write protected and unchangeable. Permalocking the EPC and User memory makes these memory banks permanently write protected and unchangeable. Users may read EPC and User memory regardless of lock status. For full details about the *Lock* command, refer to the Gen2v2 specification.

Table 4: Supported *Lock* Command Payloads for Locking Passwords

LOCK COMMAND PAYLOAD (HEX)	*LOCK* COMMAND PAYLOAD (BINARY)	*LOCK* OPERATION ACTION				TAG CHIP SUPPORTS LOCK SEQUENCE?	
		KILL PWD	ACCESS PWD	EPC MEMORY	USER MEMORY	IMPINJ M730, IMPINJ M830	IMPINJ M750, M770, M775, M780, M781, M850
F03C0	1111 0000 0011 1100 0000	Perma-locked	Perma-locked	No change	No change	Yes	Yes
A0280	1010 0000 0010 1000 0000	Locked	Locked	No change	No change	Yes	Yes
A0000	1010 0000 0000 0000 0000	Unlocked	Unlocked	No change	No change	Yes	Yes
F0140	1111 0000 0001 0100 0000	Perma-unlocked	Perma-unlocked	No change	No change	Yes	Yes
AC2B0	1010 1100 0010 1011 0000	Locked	Locked	Perma-locked	No change	Yes	Yes
A82A0	1010 1000 0010 1010 0000	Locked	Locked	Locked	No change	Yes	Yes
F83E0	1111 1000 0011 1110 0000	Perma-locked	Perma-locked	Locked	No change	Yes	Yes
FCFF3	1111 1100 1111 1111 0011	Perma-locked	Perma-locked	Perma-locked	Perma-locked	No	Yes
F8BE2	1111 1000 1011 1110 0010	Perma-locked	Perma-locked	Locked	Locked	No	Yes
A8AA2	1010 1000 1010 1010 0010	Locked	Locked	Locked	Locked	No	Yes
A8000	1010 1000 0000 0000 0000	Unlocked	Unlocked	Unlocked	Unlocked	Yes	Yes

*Note: Users can only issue a Lock command to a tag in the **secured** state. Additional valid configuration options are not listed above. If one of the fields was previously permalocked or permaunlocked, that lock status cannot be changed, and the Lock command will fail.*

2.2.2.1 Locking Tag Memory Examples

Below are examples of how to lock Impinj M700 series and M800 series tags using payloads shown in Table 4.

Example 1: Encode an Impinj M700 series and M800 series tag with a unique access password, unique EPC, lock passwords and permalock EPC memory.

- Write non-zero access password to the tag at Reserved memory words 2
- Write EPC to desired value
- Lock tag with *Lock* command with payload of $AC2B0_h$[1]

Access and kill passwords are locked and are readable or writable from the **secured** state but not from the **open** state. EPC memory is permanently locked and is not writable from **open** or **secured** state.

Example 2: Encode an Impinj M700 series and M800 series tag with a unique access password, unique EPC, permalock passwords and lock EPC memory.

- Write non-zero access password to the tag at Reserved memory words 2
- Write EPC to desired value
- Lock tag with *Lock* command with payload of $F83E0_h$

Access and kill passwords are permanently locked and are not readable or writable from **open** or **secured** state. EPC memory is locked and is writable from the **secured** state but not from the **open** state.

2.2.3 Encoding User Configurable Feature Bits

2.2.3.1 Unkillable Bit (M770 and M775 Only)

Unkillable mode prevents the killing of the tag in support of the Protected Mode feature.

All Impinj M700 series and M800 series tags support Gen2v2 password-based kill by default. However, Impinj M770 and M775 tag chips have the capability to make the tags unkillable using the Unkillable mode. This mode allows tags to be made unkillable even if the tag has a non-zero valued kill password. The access and kill passwords are shared for all Impinj M700 series and M800 series tag chips, so this mode allows tags to be password protected with a non-zero access password while preventing the tag from being killed with the same non-zero kill password.

Unkillable mode is enabled by writing the Unkillable bit to 1 in Reserved memory. This bit may be changed from the **secured** state with a zero or non-zero password. If this bit is written to a value of 1, the tag is permanently put into Unkillable mode: the bit cannot be changed, and the tag will be permanently unkillable.

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[1] From the Gen2v2 specification, after tags are inventoried, they will transition to the **secured** state if the tag has a zero-value access password. A factory default tag with a zero-value access password may have the password written and tag locked without use of the *Access* command if the tag is not re-inventoried after the password is written. If the tag is inventoried after it has a non-zero-value access password, the *Access* command sequence must be used to transition the tag from the **open** to **secured** state. The tag must be in the **secured** state to lock the tag with the *Lock* command, write a locked EPC, read a locked access or kill password.

This bit is at Reserved memory bit location 4C*h* for Impinj M770 and Impinj M775 and marked UK in the memory map.

See Impinj M770 and M775 datasheets for operational details.

Table 5: Writing the Unkillable Bit for Impinj M770 and M775, 4C*h* in Reserved memory

PAYLOAD (HEX)	PAYLOAD (BINARY)	UNKILLABLE BIT, UK	COMMENTS
0000	0000 0000 0000 **0**000	0	Default value. Tag is killable.
0008	0000 0000 0000 **1**000	1	Tag is unkillable

2.2.3.2 Memory Select Bit (M830 and M850 Only)

Memory Select Bit enables user to switch between M830 and M850 memory maps one time. This bit is at Reserved memory bit location 4C*h* in Impinj M830 and M850 and marked M in the memory map. The Impinj M830 and M850 are electrically identical chips with different default memory map selections set at the factory:

- Impinj M830 has a default M bit value of one, which selects the memory map with 128 bits of EPC memory and no User memory. Refer to datasheet for memory map details.
- Impinj M850 has a default M bit value of zero, which selects the memory map with 96 bits of EPC memory and 32 bits of User memory. Refer to datasheet for memory map details.

Table 6: Writing the Memory Map Bit for Impinj M830 and M850, 4C*h* in Reserved memory

NO TABLE OF FIGURES ENTRIES FOUND.	PAYLOAD (BINARY)	MEMORY MAP BIT, M	COMMENTS
0000	0000 0000 0000 **0**000	0	The M bit is set to the Impinj M850 memory map, with 96 bits of EPC memory and 32 bits of User memory.
0008	0000 0000 0000 **1**000	1	The M bit is set to the Impinj M830 memory map, with 128 bits of EPC memory and no User memory.

The M bit may be written only once from the secured state. The value may be permanently locked by re-writing the default value or changed only one time from zero to one (for the M850) or from one to zero (for the M830) to select the other memory map. After the memory map selection bit is written, it is locked and may not be changed again. In addition, if any valid Lock command is issued to the tag, the memory map selection bit will be permanently locked.

Note: The value of the M bit does not affect the Model Number in the TID, which is fixed.

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