Datasheet

IMPINJ M830/M850 SERIES TAG CHIPS

IPJ-M830A-A00

IPJ-M850A-A00

1 OVERVIEW

Impinj® M800 series RAIN tag chips deliver exceptional readability, inventory speed, range, decluttering, and data and privacy protection for next-generation, universal RAIN tags. The M800 series provides exceptional readability in large tag populations, on densely packed items, and on traditionally hard-to-read items such as those containing liquids and metals. Built on proven Impinj technology, the M800 series also includes Impinj Gen2X features that unlock advanced functionalities. Impinj's M800 series tag chips are truly the future of RAIN-enabled item visibility.

The M800 series comprises the Impinj M830 and M850 tag chips, with memory maps as shown below. Both chips follow the RAIN radio standard (GS1 Gen2V2, standardized as ISO/IEC 18000-63). They also support Impinj Gen2X, an enhancement to Gen2's radio and logical layers to speed inventory, increase tag read range, declutter the environment, protect consumers, inhibit label and item counterfeiting, and reduce solution cost. Gen2X interoperates seamlessly with Gen2.

With Impinj AutoTune™ adaptive tuning, the M830 and M850 further boost performance so that large and small antenna designs meet enterprise requirements. Additionally, Impinj Enduro™ V2 bonding pads strengthen chip-to-antenna adhesion, providing exceptional mechanical stability, assembly consistency, reliability, and durability over a tag's lifespan. The M830 and M850 are also drop-in compatible with Impinj M700 series antennas, enabling quick time-to-market.

1.1 Impinj M800 Series Specifications Summary

- –25.5 dBm read sensitivity with a dipole antenna and, with Impinj Power Boost, up to –27.5dBm
- –20dBm write sensitivity with a dipole antenna
- 96-bit TID with 48-bit serialization
- Two user-selectable memory maps:
  - M830: 128 bits EPC memory, 0 bits user memory
  - M850: 96 bits EPC memory, 32 bits user memory
- ISO/IEC 18000-63:2015 and GS1 Gen2v2 compliant
- Impinj Gen2X for improved solution performance and protection

1.2 Impinj M800 Series Features Summary

M800 tag chips are a key element of the Impinj platform, a foundation for RAIN solutions. They support Impinj Gen2X Performance enhancements that improve reader sensitivity, increase inventory speed, improve tag power delivery, declutter tag populations, and reliably filter those populations while reducing cost. M800 tag chips also support Gen2X Protection enhancements that protect tag data, authenticate tag chips, and protect consumer privacy.

This document includes some Gen2X features but does not specify the entirety of Gen2X. For more information on Gen2X, please request support through the Impinj Support Portal at support.impinj.com.

1.2.1 Impinj M800 Performance Enhancements

M800 tag chips operate seamlessly in Gen2 or Gen2X inventory rounds. Gen2X improves tag readability, especially for small tags on densely packed items. In mixed tag populations, readers alternate Gen2 and Gen2X inventory rounds to read all tags. Regardless of the population mix, Gen2X consistently improves solution performance. The M800 series boasts improved:

- **Reader sensitivity:** Improved Gen2X preamble, backscatter modulation, pilot tone, and symbol encoding improve tag-to-reader waveform Eb/N0 by up to 7.5dB.
- **Inventory speed:** Configurable Gen2X RN16 parameters accelerate inventory by reducing *ACK* data and erroneous *ACK*s. Impinj TagFocus™, available in both Gen2 and Gen2X inventory rounds, allows a reader to reduce re-inventory time and focus on new tags.
- **Power delivery:** Powerup waveform shaping and extended Tari values allow readers to deliver more power to tags, improving tag sensitivity up to 2 dB in both Gen2 and Gen2X inventory rounds.

- **Tag decluttering:** Session-dependent Gen2X RN16 protection allows readers to discriminate which reader a tag's response is intended for, reducing cross-reads in multi-reader environments. Session-flag Booleans, available in both Gen2 and Gen2X inventory rounds, provide readers with advanced tag decluttering techniques.
- **Tag filtering:** Tag selection during Gen2X inventory-round initiation ensures only tags-of-interest participate. Configurable Gen2X inventory response (TID or EPC) allow TID-based solutions.
- **Impinj AutoTune™ V3:** Tag chip self-tuning improves tag readability across materials, form factors, and reader RF frequencies by tuning the tag chip to optimize RF energy harvesting in both Gen2 and Gen2X inventory rounds.

1.2.2 Impinj M800 Protection Enhancements

M800 tag chips protect data, enable authentication, and protect consumer privacy. These protection features are part of Gen2X Protection but are also available during Gen2 inventory rounds.

- **Protecting tag data:** The M800 series includes on-chip memory integrity checks, execution checks that prevent an M800 chip from sending a corrupted EPC, and a reader command that validates the data stored in chip memory. These features are collectively called Impinj Integra™.
- **Authenticating tag chips:** The M800 series includes Impinj FastID™ for rapid EPC+TID inventory and EPC ⇔ TID verification (Gen2 only). Impinj Protected Mode™ (PIN-protected reversible kill) inhibits fraudulent product returns.
- **Protecting privacy:** Protected Mode protects consumer privacy by turning an M800 nonresponsive to a reader unless the reader first provides a correct PIN. Short-range mode reduces tag read range by roughly 10× (20 dB).

1.2.3 Additional Impinj M800 Series Features

M800 tag chips include additional features beyond performance and protection, including:

- **Impinj Enduro™ V2**: Strengthens the chip-to-antenna connection to improve tag performance, reduce performance variation and ensure tag durability and reliability.
- **Impinj Self-Serialization:** Enables reliable and scalable inlay encoding by generating unique SGTIN serialization directly from a tag chip's TID.
- **User-Selectable Memory Map:** Allows inlay manufacturers to configure an M800-series chip to either the M830 or M850 memory map.

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2 INTRODUCTION

2.1 Scope

This datasheet provides the physical and logical specifications for Impinj M800 series RAIN tag chips.

2.2 Reference Documents

The following reference documents are used in this datasheet:

- EPC™ Radio-Frequency Identity Protocols Generation-2 UHF RFID Protocol for Communications at 860 MHz – 960 MHz (Gen2v2 Protocol), V2.1.0, Jul 2018
  - This datasheet uses the conventions in the Gen2V2 protocol (normative references, terms and definitions, symbols, abbreviated terms, and notation). Users of this datasheet should familiarize themselves with the Gen2v2 protocol.
- Impinj M830 and M850 Wafer Specification
- Impinj Wafer Map Orientation Guide
- TID Memory Maps for Impinj Monza Self-Serialization Application Note
- Impinj Tag Quieting Application Note
- EPC™ Tag Data Standard (TDS) Release 2.0, Aug 2022
- Interoperability Test System for EPC Compliant Class-1 Generation-2 UHF RFID Devices Release.2.0.1, Feb 2016

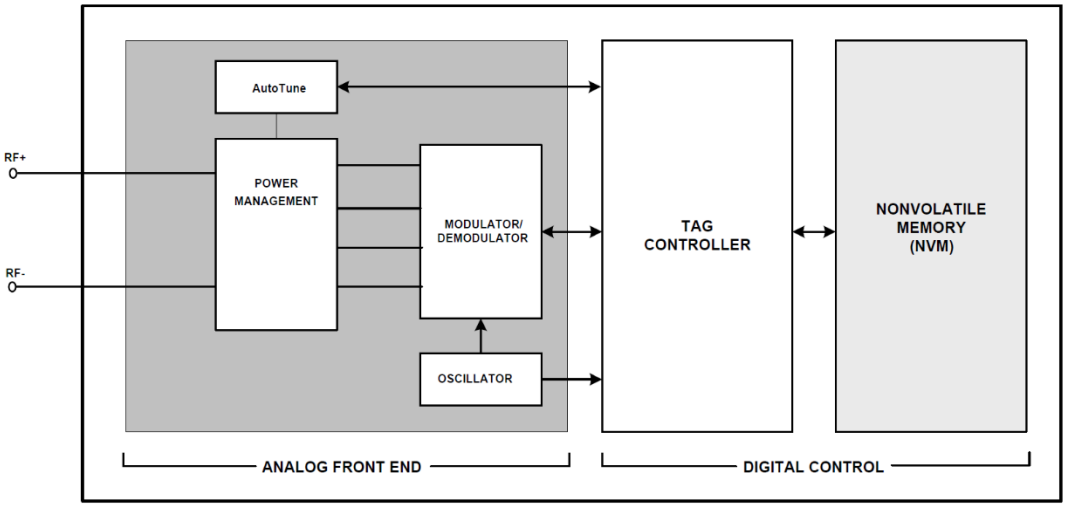
Consult these documents for more information about compliance standards and specifications.

3 FUNCTIONAL DESCRIPTION

M800 tag chips support all mandatory commands of the Gen2v2 protocol and some of its optional commands and features (see Optional Gen2v2 Commands, section 3.2).

3.1 Impinj M800 Tag Chip Block Diagram

Figure 1: Block Diagram



3.1.1 Power Management

A tag is powered by a RAIN reader's RF field. When the tag enters the reader's RF field, the Power Management block converts RF field energy to a DC voltage that powers the chip.

3.1.2 AutoTune™

The AutoTune block improves power harvesting from the inlay antenna by automatically tuning the chip's input capacitance. Compared with earlier Impinj chips, the M800's tuning algorithm improves symmetry around tag resonance and widens the tuning dynamic range across the entire 860–960 MHz spectrum. AutoTune adjustment occurs at chip power-up. For information on how to read AutoTune values or configure AutoTune, refer to the Reserved Memory section of this document.

3.1.3 Modulator/Demodulator

The modulator/demodulator block modulates tag replies and demodulates reader commands. An M800 sends data to a reader by modulating the reflection coefficient of its antenna ports between reflective and absorptive states. The data are encoded as either Gen2V2 FM0 or Miller subcarrier or Gen2X BPSK subcarrier (the reader specifies the encoding choice and data rate). For reader-to-tag communications, M800 tag chips demodulate all Gen2V2 data formats: DSB-ASK, SSB-ASK or PR-ASK, all with PIE encoding. Gen2X uses the same reader-to-tag data formats.

3.1.4 Tag Controller

The Tag Controller block is a finite state machine (digital logic) that executes command sequences and controls memory operations.

3.1.5 Nonvolatile Memory

The Nonvolatile Memory (NVM) block uses an Impinj-invented memory technology optimized for RAIN applications, providing 10,000 write cycle endurance or 10-year data retention. The memory write speed is 2.9 ms per 32 bits for *Write*, *BlockWrite*, *Lock* or *Kill* operations.

The M800 memory is organized into the four banks specified in Gen2V2:

- Reserved: Includes access and kill passwords as well as feature and chip control words
- EPC: 128 bits for M830; 96 bits for M850
- TID: Contains the $E2_h$ ISO/IEC 15963 class-identifier value, Impinj mask-designer identifier (000000001_b) and the M800 model number. It also includes an extended TID comprising a 16-bit header and 48-bit serialization. The TID and the extended TID are programmed and permalocked at manufacturing and are read-only.
- User: 0 bits for M830; 32 bits for M850

Table 1: Impinj M800 Series Memory Organization

Memory Section	M830	M850
EPC	128 bits	96 bits
User	0 bits	32 bits
TID (not changeable)	48-bit serial number	48-bit serial number
	16-bit extended TID Header	16-bit extended TID Header
	32-bit TID precursor (see Gen2V2)	32-bit TID precursor (see Gen2V2)
Reserved	Chip configuration	Chip configuration
	32-bit Kill/Access password (shared)	32-bit Kill/Access password (shared)

3.2 Optional Gen2v2 Commands

M800 tag chips support the optional commands in Table 2 below, in both Gen2 and Gen2X inventory rounds. Refer to Gen2v2, version 2.1.0, for further details on these commands.

Table 2: Supported Gen2v2 Protocol Commands

Command	Details
Access	• Supports full *Access* command memory-access functionality
BlockWrite	• Accepts one-word (16-bit) *BlockWrites*; accepts two-word (32-bit) *BlockWrites* if pointer has an even value • Returns error code “Not Supported” (00000001_b) upon receiving a two-word *BlockWrite* with an odd pointer or a BlockWrite specifying more than two words • Does not respond to *BlockWrite* commands specifying zero words
Lock	• Separately (perma)lockable EPC and User memory banks (the TID memory bank is factory permalocked and therefore not lockable) • (Perma)lockable Access / Kill password. These passwords have the same value, share their lock status and cannot be locked independently from each other. For further details on locking the shared password, see section 4.8.1.3
Untraceable	• Supports the Range parameter to switch between short and maximum operating range. Allows temporarily toggling read range as specified in Gen2V2. See section 4.8.2 for an alternative method to put an M800 into short-range mode • Does not support EPC shortening. The EPC length field (**L** bits) in the *Untraceable* command must match the EPC length (**L**) bits in the StoredPC word (10_h – 14_h)

3.3 Impinj Integra™ V2 Memory Diagnostics

The RAIN standard does not include memory integrity requirements nor specify how a chip manufacturer should ensure data integrity. Instead, it empowers chip manufacturers to decide for themselves how to meet market requirements for data integrity, in a similar fashion to other industries where memory suppliers develop and use their own approaches for memory data integrity.

M800 tag chips provide improved memory diagnostics and data integrity checks that both minimize data errors and allow readers to check the data stored in the chip’s memory. These features include memory self-check and an Impinj *MarginRead* command. They are available in both Gen2 and Gen2X inventory rounds.

3.3.1 Memory Self-Check

Memory errors are rare but can occur, such as from cosmic rays, chip damage, temperature excursions or latent chip defects. M800 self-check automatically protects against memory errors by performing an automatic word-wise parity check on all memory words. If the automatic memory checking detects an error it prevents tags from sending corrupted data to a reader.

3.3.1.1 TID and Reserved Memory Check

At power-up, an M800 checks Reserved memory words 4 and 5 and in TID memory words 0 – 5. It does not send any response to any command if a check of any of these words fails. If the chip sends an RN16 in response to a *Query* command then the Reserved and TID check has passed.

3.3.1.2 EPC Check

At power-up, an M800 checks its EPC, with length specified by the **L** bits in the StoredPC, for errors. It sends a zero-length EPC if it detects an EPC error. It sends a zero-length EPC and an inverted PacketCRC if it detects a StoredPC error. It sends the expected EPC and PacketCRC if there are no errors.

3.3.1.3 Read Memory Check

Upon receiving a *Read* command, an M800 checks the requested data for errors. It sends the requested data and an inverted CRC if it detects an error. It sends the requested data if there are no errors.

3.3.1.4 Shared Password Check

Upon receiving a *Kill* or *Access* command sequence, an M800 checks the shared password for errors. If it detects an error, the chip will not enter the **killed** or **secured** state and will send the error code shown below. If there is no password error, it performs as expected.

- *Kill* command sequence: A chip with a password error sends error code 00000000_b (i.e. as if the kill password was zero-valued).
- *Access* command sequence: A chip with a password error sends error code 00000000_b (i.e. as if the access was disallowed).

3.3.1.5 Recommended Memory Self-Check Usage

Readers can easily screen memory errors because M800 chips self-report issues.

- If inventory rounds or read operations complete successfully, the chip didn't detect errors.
- If *Access* or *Kill* operations complete successfully, the chip didn't detect errors.
- If an M800 does detect an error, it will notify the reader as described above.

3.3.2 *MarginRead* Command

MarginRead is a custom Impinj command that allows a reader to verify that each NVM bit has sufficient margin for reliable operation. It improves encoding quality control and aids NVM failure analysis.

Table 3, Table 4 and Table 5 provide *MarginRead* command details.

Table 3: *MarginRead* Command Details

Command	Code	Length	Details
MarginRead	11100000 00000001	≥ 67 bits	• An M800 must be in the open or secured state to execute a *MarginRead* • If an M800 receives a *MarginRead* with an invalid Handle then it ignores the command • If an M800 doesn't have sufficient power to execute a *MarginRead* then it responds with an Insufficient Power error code • If the any bit in the memory range specified by Pointer and Length has insufficient write margin or mismatches Mask then an M800 responds with an Other Error code • An M800 will only perform *MarginRead* on programmable NVM bits and will ignore all Mask bits that correspond to non-programmable NVM bits.

Table 4: *MarginRead* Command Code

MarginRead Command	Code	Mem Bank	Pointer	Length	Mask	RN	CRC-16
#bits	16	2	EBV	8	Variable	16	16
Details	11100000 00000001	00: Reserved 01: EPC 10: TID 11: User	Starting Bit Address Pointer	Length in Bits	Mask Value	Handle	CRC-16

Table 5: *MarginRead* Command Field Descriptions

Field	Description
Mem Bank	The memory bank to access
Pointer	An EBV that indicates Mask starting bit address
Length	Mask length (1 – 255 bits). An M800 ignores *MarginRead* commands with Length=0
Mask	The values the reader expects an M800 to have in the memory cells specified by Pointer and Mask.
RN	An M800 will ignore a *MarginRead* with an invalid Handle

An M800 responds to a *MarginRead* using the preamble specified by the TRext value in the *Query* or *Scan* that initiated the round. See Table 6 for M800 response details.

Table 6: Tag Response to a Passing *MarginRead* Command

Response	Header	RN	CRC-16
Description	0_b	16-bit Handle	CRC-16

3.3.3 Recommended *MarginRead* Usage

There are many ways to use a *MarginRead* with M800 tag chips. M800 is factory EPC pre-serialized at the factory; a *MarginRead* allows a reader to verify that the pre-serialized data are written correctly and do not need to be re-encoded. Another use of *MarginRead* is verifying field data encoding. *MarginRead* can also be used to diagnose and analyze tag memory failures.

3.4 Impinj Protected Mode Privacy Protection

Impinj Protected Mode is effectively a reversible kill. It protects consumer privacy by turning an M800 nonresponsive to a reader unless the reader first provides a correct 32-bit PIN. Protected Mode also protects against fraudulent product returns because the person returning the product must supply the correct PIN to turn the M800 responsive again. Protected Mode is available in both Gen2 and Gen2X inventory rounds.

For more information on Protected Mode in M800 tag chips, please request support through the Impinj Support Portal at support.impinj.com.

3.5 Impinj TagFocus™ Read Redundancy Prevention

TagFocus allows readers to silence already-inventoried M800 chips by refreshing the chips' S1 flag B state persistence. TagFocus reduces redundant reads, allowing a reader to focus on weak tags that are typically the last to be found. TagFocus is available in both Gen2 and Gen2X inventory rounds.

For more information on TagFocus in M800 tag chips, please request support through the Impinj Support Portal at support.impinj.com.

3.6 Impinj FastID™ EPC+TID Reading

FastID allows readers to instruct M800 chips to concatenate their TID with their EPC during inventory, speeding TID reading by avoiding the lengthy access / read sequence. Setting the EPC word length to zero enables TID-only inventory. FastID is available only in Gen2 inventory rounds. For Gen2X rounds, the *Scan* commands have provisions for EPC response, TID response or both.

For more information on enabling FastID in M800 tag chips, please request support through the Impinj Support Portal at support.impinj.com.

3.7 Impinj Power Boost and Extended Tari

Power Boost is an improved reader powerup waveform that delivers up to 2dB additional power to M800 chips during powerup initialization, when they most need it. This additional initialization power increases overall M800 operating sensitivity by up to a commensurate 2dB. Extended Tari values further increase available power during reader commands. Power Boost and extended Tari values are available in both Gen2 and Gen2X inventory rounds.

For more information on enabling Power Boost and extended Tari values in M800 tag chips, please request support through the Impinj Support Portal at support.impinj.com.

3.8 Impinj Tag Quieting

Tag quieting allows readers to perform Boolean operations on M800 session and select flags to silence already-inventoried tag subpopulations and thereby declutter complex enterprise tag environments. Tag quieting is available in both Gen2 and Gen2X inventory rounds.

For more information on enabling Tag Quieting in M800 tag chips, please request support through the Impinj Support Portal at support.impinj.com.

3.9 Impinj Gen2X Inventory Rounds

M800 tag chips operate seamlessly across Gen2 and Gen2X inventory rounds. In mixed chip populations, with readers alternating between Gen2 and Gen2X inventory rounds, M800 tag chips will participate in both. Regardless of the population mix, Gen2X consistently improves solution performance.

To initiate a Gen2 inventory round, a reader sends a Gen2 preamble followed by a *Query* command, and for a Gen2X inventory round, a reader sends a Gen2X preamble followed by a *Scan* command. The reader controls whether subsequent inventory rounds are Gen2 or Gen2X by sending a *Query* or *Scan*, respectively. M800 chips share session and select flag values across Gen2 and Gen2X inventory rounds, allowing seamless tag population management across Gen2 and Gen2X.

All other reader commands are the same between Gen2 and Gen2X, but the frame-syncs are different. Gen2 inventory rounds use a Gen2 frame-sync whereas Gen2X inventory rounds use a Gen2X frame-sync. When in a Gen2 inventory round, M800 tag chips ignore commands with a Gen2X frame sync, and vice versa. All commands except *Query* and *Scan* are common between Gen2 and Gen2X inventory rounds – the only difference is the frame-sync.

Regardless of inventory round type, M800 tag chips accept *Select* and *Challenge* commands preceded by either a Gen2 frame sync or Gen2X frame-sync.

For more details on Gen2X inventory rounds please request support through the Impinj Support Portal at support.impinj.com.

3.9.1 Tag-to-Reader Link Enhancements

M800 tag chips, in Gen2X inventory rounds, use more modern radio techniques to communicate back to a reader. These techniques include an improved preamble, antipodal (BPSK) encoding, an optional extended pilot tone and forward-error-correction (FEC) symbol encoding that improve waveform Eb/N0 by up to 7.5dB.

Other Gen2X link enhancements include configurable RN16 parameters, both numerical and error-reducing, that accelerate inventory by reducing *ACK* data and erroneous *ACK*s. They also include session-dependent RN16 protection that allows readers to discriminate which reader a tag's response is intended for, reducing cross-reads in multi-reader environments.

For more details on Gen2X tag-to-reader link enhancements, please request support through the Impinj Support Portal at support.impinj.com.

3.10 Antenna Input

M800 tag chips have two external Enduro V2 pads: RF+ and RF–, as shown in Table 7. Figure 2 shows the two pads, which are gold-coated. These pads form the M800's antenna port. All external interaction with an M800 series tag chip, including power generation and signaling, occurs via the antenna port. **Error! Reference source not found.** shows the antenna connections. Note that neither pad connects to the chip substrate.

Table 7: Pad Descriptions

External Signals	External Pad	Description
RF+	1	Differential RF input pads
RF–	2	

Figure 2: Impinj M800 Series Tag Chip

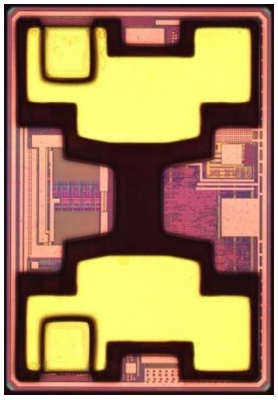
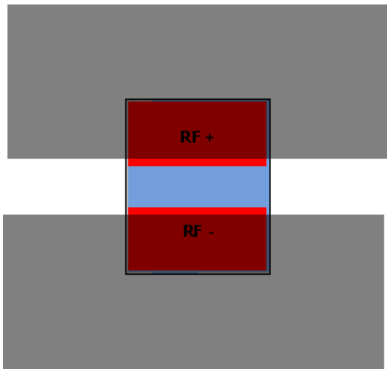


Figure 3: Antenna Connection for Inlay Production



3.11 Impinj M800 Series Antenna Reference Designs

M800 tag chips are drop-in compatible with M700 antenna designs, although antenna optimization may further improve performance. Impinj has M800 antenna reference designs available under the terms of the Impinj Antenna License Agreement. To access these reference designs, users obtain permission by first creating an Impinj access account and then submitting a request form through the Impinj Partner Access page. After Impinj has accepted the request, users can use their access credentials to view the Impinj Endpoint IC reference design documents page on the Support Portal.

3.12 Impinj M800 Series Tag Chip Dimensions

The M830 and M850 chip dimensions are:

- 362.0µm × 247.0µm die size
- 109.5µm × 215.0µm pad size
- 111.0µm pad spacing at the chip center
- 187.2µm pad spacing at the chip edge

4 INTERFACE CHARACTERISTICS

This section describes the M800's RF interface and the modulation characteristics of the reader-to-tag (Forward Link) and tag-to-reader (Reverse Link) communication links.

4.1 Antenna Connections

Error! Reference source not found. shows the antenna connections for M800 tag chips. One antenna terminal connects to the RF+ Enduro pad and one to the RF– pad. The antenna traces should partially overlap the pads but not extend into the gap between the pads.

4.2 Impedance Parameters

To maximize the performance of M800-based inlays, an antenna should present a proper impedance to the chip. The simplified lumped-element tag chip model shown in Figure 4 is the conjugate of the ideal source impedance, but note that it is *not* equal to the chip's input impedance. Impinj uses an indirect, source-pull method for deriving the port impedance model, made necessary by the nonlinear, time-varying nature of the tag's RF circuits. This model provides a good mathematical fit over a broad frequency range.

The lumped element values are listed in Table 8. C_{mount} is the parasitic capacitance from the antenna trace overlap with the chip surface. C_p is at the chip terminals and is intrinsic to the chip. R_p represents the energy conversion and absorption of the chip's RF circuits. This model applies to all frequencies in the primary regions of operation (including North America and Europe).

Figure 4: Tag Chip Linearized RF Model

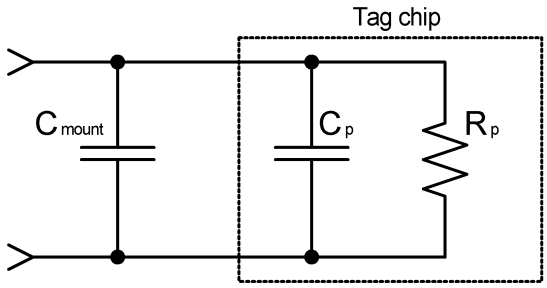


Table 8: Impinj M800 Series RF Parameters

Parameter	Typical Value	Comments
R_p	3.50 kΩ	Calculated for linearized RF model shown in Figure 4.
C_p	0.930 pF	Intrinsic chip capacitance when AutoTune is mid-range, including Enduro pads.
C_{mount}	0.115 pF	Typical capacitance due to adhesive and antenna mount parasitic effects[1]
Total Load Capacitance	1.045 pF	Total load capacitance presented to antenna model of Figure 4 is C_p + C_{mount}
Read Sensitivity	– 25.5 dBm	Measured in a 50-ohm system using a response to a *Query* command with a +2.15 dBi dipole.
Write Sensitivity	– 20.0 dBm	

[1] For modeling purposes only.

4.3 Reader-to-Tag (Forward Link) Signal Parameters

Table 9: Forward Link Signal Parameters – RF Parameters

Parameter	Minimum*	Typical	Maximum*	Units	Comments
Carrier Frequency	860		960	MHz	North America: 902–928 MHz Europe: 865–868 MHz
Maximum RF Field Strength			+20	dBm	Received by the chip
Modulation		DSB-ASK, SSB-ASK, PR-ASK			Double and single sideband amplitude shift keying; phase-reversal amplitude shift keying
Data Encoding		PIE			Pulse-interval encoding
Modulation Depth	80		100	%	(A-B)/A, A=envelope max., B=envelope min.
Ripple, Peak-to-Peak			5	%	Portion of A–B
Rise Time (tr,10–90%)	0		0.33Tari	sec	
Fall Time (tf,10–90%)	0		0.33Tari	sec	
Gen2V2 Tari*	6.25		25	µs	Data 0 symbol period
Gen2X Tari*	6.25		40	µs	Data 0 symbol period
PIE Symbol Ratio	1.5:1		2:1		Data 1 symbol duration relative to Data 0
Duty Cycle	48		82.3	%	Ratio of data symbol high time to total symbol time
Gen2V2 Pulse Width	MAX(0.265 Tari, 2)		0.525Tari	µs	Pulse width defined as the low modulation time (50% amplitude)
Gen2X Pulse Width	2.0		0.50Tari		6.25 – 11µs Tari
	3.8		min(0.50Tari, 8.0)	µs	11 – 40µs Tari

* Values are the nominal minimum and nominal maximum and do not include frequency tolerance. Apply appropriate frequency tolerance to derive absolute periods and frequencies.

For more details on signal parameters, please request support through the Impinj Support Portal at support.impinj.com.

4.4 Tag-to-Reader (Reverse Link) Signal Parameters

Table 10: Reverse Link Signal Parameters – Modulation Parameters

Parameter	Minimum*	Typical	Maximum*	Units	Comments
Modulation		ASK			
Gen2V2 Data Encodings		FM0 or Miller Subcarrier			
Gen2X Data Encoding		BPSK subcarrier			
Change in Modulator Reflection Coefficient $\|\Delta\Gamma\|$ due to Modulation		0.8			$\|\Delta\Gamma\| = \left\|\Gamma_{reflect} - \Gamma_{absorb}\right\|$ (per read/write sensitivity, Table 8)
Duty Cycle	45	50	55	%	
Symbol Period	1.5625		25	µs	FM0 (Gen2V2)
	3.125		200	µs	Miller subcarrier (Gen2V2)
	1.5625		200	µs	BPSK subcarrier (Gen2X)
Miller or BPSK Subcarrier Frequency*	40		640	kHz	

* Values are the nominal minimum and nominal maximum and do not include frequency tolerance. Apply appropriate frequency tolerance to derive absolute periods and frequencies.

For more details on modulation parameters, please request support through the Impinj Support Portal at support.impinj.com.

4.5 Impinj M830 Tag Chip Memory Map

Table 11: Impinj M830 Physical/Logical Memory Map

Memory Bank Number	Memory Bank Name	Memory Bank Bit Address	Bit Address															
			0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
10_2	TID (ROM)	80_h-$8F_h$	RFU															
		50_h-$5F_h$	TID_Serial [15:0]															
		40_h-$4F_h$	TID_Serial [31:16]															
		30_h-$3F_h$	TID_Serial [47:32]															
		20_h-$2F_h$	Extended TID Header = 2000_h															
		10_h-$1F_h$	MDID [3:0] = 1_h				Model Number = $1B0_h$											
		00_h-$0F_h$	1	1	1	0	0	0	1	0	1	0	0	MDID [8:4] = 00_h				
01_2	EPC (NVM)	90_h-$9F_h$	EPC [15:0]															
		80_h-$8F_h$	EPC [31:16]															
		70_h-$7F_h$	EPC [47:32]															
		60_h-$6F_h$	EPC [63:48]															
		50_h-$5F_h$	EPC [79:64]															
		40_h-$4F_h$	EPC [95:80]															
		30_h-$3F_h$	EPC [111:96]															
		20_h-$2F_h$	EPC [127:112]															
		10_h-$1F_h$	Protocol-Control Bits (PC)															
		00_h-$0F_h$	CRC-16															
00_2	RESERVED (NVM)	140_h-$14F_h$	RFU [12:0]=000_h													ATV[2:0]		
		70_h-$7F_h$	Factory Calibration C [15:0]															
		60_h-$6F_h$	Factory Calibration B [15:0]															
		50_h-$5F_h$	Factory Calibration A [15:0]															
		40_h-$4F_h$	Internal Config [15:5]											SR	M	Internal Config [2:1]		A
		30_h-$3F_h$	Shared Access Password [15:0]															
		20_h-$2F_h$	Shared Access Password [31:16]															
		10_h-$1F_h$	Shared Kill Password [15:0]															
		00_h-$0F_h$	Shared Kill Password [31:16]															

Note: M830 tag chips have a single, shared 32-bit password.

4.6 Impinj M850 Tag Chip Memory Map

Table 12: Impinj M850 Physical/Logical Memory Map

Memory Bank Number	Memory Bank Name	Memory Bank Bit Address	Bit Address															
			0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
11_2	USER (NVM)	10_h-$1F_h$	User [15:0]															
		00_h-$0F_h$	User [31:16]															
10_2	TID (ROM)	80_h-$8F_h$	RFU															
		50_h-$5F_h$	TID_Serial [15:0]															
		40_h-$4F_h$	TID_Serial [31:16]															
		30_h-$3F_h$	TID_Serial [47:32]															
		20_h-$2F_h$	Extended TID Header = 2000_h															
		10_h-$1F_h$	MDID [3:0] = 1_h				Model Number = $1B0_h$											
		00_h-$0F_h$	1	1	1	0	0	0	1	0	1	0	0	MDID [8:4] = 00_h				
01_2	EPC (NVM)	90_h-$9F_h$	EPC [15:0]															
		60_h-$6F_h$	EPC [31:16]															
		50_h-$5F_h$	EPC [47:32]															
		40_h-$4F_h$	EPC [63:48]															
		30_h-$3F_h$	EPC [79:64]															
		20_h-$2F_h$	EPC [95:80]															
		10_h-$1F_h$	Protocol-Control Bits (PC)															
		00_h-$0F_h$	CRC-16															
00_2	RESERVED (NVM)	140_h-$14F_h$	RFU [12:0]=000_h													ATV[2:0]		
		70_h-$7F_h$	Factory Calibration C [15:0]															
		60_h-$6F_h$	Factory Calibration B [15:0]															
		50_h-$5F_h$	Factory Calibration A [15:0]															
		40_h-$4F_h$	Internal Config [15:5]											SR	M	Internal Config [2:1]		A
		30_h-$3F_h$	Shared Access Password [15:0]															
		20_h-$2F_h$	Shared Access Password [31:16]															
		10_h-$1F_h$	Shared Kill Password [15:0]															
		00_h-$0F_h$	Shared Kill Password [31:16]															

Note: M850 tag chips have a single, shared 32-bit password.

4.7 Logical vs. Physical Bit Identification

Logical MSBs correspond to most significant bits and LSBs to least significant bits. For example, bit 15 is the logical MSB of a row in the memory map whereas bit 0 is the LSB. When read from left to right, a multi-bit word represented by WORD[N:0] is interpreted MSB first. This convention is distinct from the physical bit address indicated by the rows and column addresses in the memory map; the physical bit address, used for the memory bank bit addresses, describe the addressing used to access the memory.

4.8 Reserved Memory

Reserved memory contains kill and access passwords at locations 00–1Fh and 20–3Fh, respectively. For M800 chips, these passwords are shared, are constrained to have the same value and are inseparably locked and permalocked together. They are programmed to zero at the factory.

M800 tag-chip Reserved memory also contains three user configuration bits, whose value may only be changed in the **secured** state with a nonzero access password unless otherwise noted. An M800 chip transitions from the **open** to the **secured** state after receiving an *Access* command sequence with the correct access password.

- **SR** = short-range bit, at Reserved memory bit location $4B_h$. **SR** is set to 0_b at the factory. When **SR** is changed to 1_b, the chip is in short-range mode, reducing its sensitivity by roughly 10× (20dB). See section 4.8.2 for more details.
- **M** = memory map selection bit, at Reserved memory bit location $4C_h$. **M** is set to 1_b for M830 and to 0_b for M850 at the factory. An inlay provider may write **M** only once, after which the setting is permanent. See section 4.8.2 for more details.
- **A** = AutoTune disable bit, at Reserved memory bit location $4F_h$. **A** is set to 0_b at the factory. AutoTune is enabled when **A**=0_b. When **A** is changed to 1_b, AutoTune is disabled, and the chip's input capacitance takes AutoTune's mid-range value. See section 4.8.3 for more details.

To write these bits, a reader issues a *Write* or single-word *BlockWrite* to word 4 of Reserved memory. These bits must be written at the same time. Note that the **SR** and **A** bits may be changed multiple times, whereas the **M** bit can be written only once. If an inlay provider wishes to change the **M** value, they must do so at the first write to word 4 of Reserved memory. When writing to word 4, use the payloads shown in Table 13.

When reading the AutoTune value, marked **ATV**[2:0] in word 14_h, the chip will reply with its current tuning capacitance value between zero and four.

Table 13: Writing User Configurable Bits, Word 4_h of Reserved Memory

Payload (Hex)	Payload (Binary)	Short-range Bit, SR	Memory Map Bit, M	AutoTune Disable Bit, A	Comments
0000	0000 0000 000**0** **0**00**0**	**0**	**0**	**0**	Default values. Chip sensitivity is max; AutoTune is enabled. **M** is set to the M850 memory map (96-bit EPC, 32-bit User memory).
0008	0000 0000 000**0** **1**00**0**	**0**	**1**	**0**	Default values. Chip sensitivity is max; AutoTune is enabled. **M** is set to the M830 memory map (128-bit EPC , zero User memory).
0010	0000 0000 000**1** **0**00**0**	**1**	**0**	**0**	Chip sensitivity is reduced. AutoTune is enabled. **M** is set to the M850 memory map (96-bit EPC, 32-bit User memory).
0001	0000 0000 000**0** **0**00**1**	**0**	**0**	**1**	Chip sensitivity is max; AutoTune is disabled. **M** is set to the M850 memory map (96-bit EPC, 32-bit User memory).
0011	0000 0000 000**1** **0**00**1**	**1**	**0**	**1**	Chip sensitivity is reduced. AutoTune is disabled. **M** is set to the M850 memory map (96-bit EPC, 32-bit User memory).

Note: This word must be written in the **secured** state. To change the **SR** bit, the chip must also have a nonzero access password and must enter the **secured** state must using the *Access* command. The **M** bit may be written only once – after it is written, the word can be rewritten, but the **M** bit value will not change.

4.8.1 Shared Access and Kill Password

M800 tag chips have a shared 32-bit password for *Access* and *Kill*. Writing (*Write* or *BlockWrite*) or locking (*Lock*) one password will write or lock the other. Said another way, the shared password may be read, written or locked from either the kill or access password memory address. Multi-row reads of the Reserved memory bank will return the same password for words 0–1 and 2–3. M800 chips will respond to *Access*, *Kill* and *Lock* commands as if the access and kill passwords are logically independent, even though they share the same physical memory and modifying one inherently modifies the other. The default value for the shared password is zero.

4.8.1.1 Access Password

The single, shared 32-bit password functions as the access password in Reserved memory 20_h to $3F_h$, MSB first. The default value is zero. Chips with a nonzero access password require that a reader send this password in an *Access* sequence before transitioning to the **secured** state. The password in the access password location always has the same value and lock status as the kill password.

4.8.1.2 Kill Password

The single, shared 32-bit password functions as the kill password in Reserved Memory 00_h to $1F_h$, MSB first. The default value is zero. Chips with a nonzero kill password require that a reader send this password as part of a *Kill* sequence before permanently transitioning to the **killed** state. Chips in the **killed** state do not respond to any commands. A chip will not execute a kill if its kill password is zero.

4.8.1.3 Locking the Shared Password

Because M800 series tags use a shared password for access and kill, the passwords lock and unlock together. The table below lists examples of *Lock* command payloads for locking this password.

Note that a single *Lock* command can lock additional memory with the passwords, as long as the access and kill password lock parameters have the same value. If a *Lock* command payload is invalid then an M800 will respond with an error code “Not supported” (00000001_b). Refer to the Gen2V2 protocol for details about the *Lock* command.

Table 14: Supported *Lock* Command Payloads for Locking Passwords

Lock Command Payload (Hex)	Lock Command Payload (Binary)	Description
A0000	1010 0000 0000 0000 0000	Access and kill passwords are unlocked and are readable or writable from the **open** or **secured** states.
F0140	1111 0000 0001 0100 0000	Access and kill passwords are permanently unlocked and are readable or writable from the **open** or **secured** states.
A0280	1010 0000 0010 1000 0000	Access and kill passwords are locked and are readable or writable from the **secured** state but not from the **open** state.
F03C0	1111 0000 0011 1100 0000	Access and kill passwords are permanently locked and are not readable or writable from any state.

4.8.2 Short-range Mode

M800 tag chips can reduce their read range by roughly 10× (20dB) to protect consumer privacy. A reader puts an M800 into short-range mode by either writing the short-range bit (**SR**) in Reserved memory or using an *Untraceable* command.

SR operation: A reader writes **SR** for an M800 in the **secured** state with a nonzero access password.

- The factory-programmed **SR** value is zero, meaning the tag operates at maximum range.
- To enable short range, a reader writes **SR** to one.
- To enable long-range, a reader writes the **SR** bit back to zero.

Refer to Table 13 for an example of ways to configure bits in Reserved memory.

***Untraceable* operation:** A reader sends a Gen2v2 *Untraceable* command, specifying range as described below, to an M800 in the **secured** state with a nonzero access password.

- If range is set to 10_b: An M800 will set **SR** to 1_b.
- If range is set to 00_b: An M800 will set **SR** to 0_b.
- If range is set to 01_b: the **SR** value will not change but the M800 will operate as is the **SR** value was inverted. For example:
  - If an M800, operating at normal range with **SR** = 0_b, receives an *Untraceable* with range = 01_b, then it will transition to short-range operation until it loses power. A reader can use this feature to ensure it can communicate with the M800 at short range before committing a persistent **SR** value to memory.

4.8.3 Memory Map Selection

The memory map selection bit, marked **M** in the memory map, is in Reserved word 4_h. The M830 and M850 are electrically identical chips with different default memory maps set at the factory:

- M830 has a default **M** value of 1_b, which selects the memory map with 128 bits of EPC memory and no User memory. Refer to Table 11 for memory map details.
- M850 has a default **M** value of 0_b, which selects the memory map with 96 bits of EPC memory and 32 bits of User memory. Refer to Table 12 for memory map details.

An M800 allows a reader to write its **M** bit only once, from the **secured** state. An inlay provider should always write (i.e. permanently lock) the **M** bit to prevent subsequent changes. A reader can retain the as-delivered memory map by rewriting the as-delivered **M** value, or can change the memory map by writing the alternative **M** value. Also note that an M800 permanently locks its **M** value upon receiving any valid *Lock* command. So, for example, if an M800 with an unlocked **M** bit receives a *Lock* to permanently lock the EPC, if will lock its **M** bit at the same time.

Note: The **M**-bit value does not affect the TID Model Number, which is fixed.

4.8.4 AutoTune Disable and AutoTune Value

M800 AutoTune allows a reader to (1) disable AutoTune functionality or (2) read the AutoTune state from memory. The AutoTune disable bit, marked **A** in the memory map, is in word 4_h of Reserved memory. The AutoTune state, marked **ATV**[2:0] in the memory map, is in word 14_h of Reserved memory.

ATV indicates an M800's tuned input capacitance. A value of zero means the chip removed 100 fF from its input at powerup. A value of four means the chip added 100 fF to its input at powerup. See Table 15 for the mapping between **ATV** and change in input capacitance. A reader reads the ATV value by issuing a single-word *Read* command to word 14_h of Reserved memory. **ATV** is not writable.

- The factory programmed **A** value is 0_b, enabling AutoTune by default.
- To disable AutoTune, a reader writes **A** to 1_b. When AutoTune is disabled, the chip sets its input capacitance to midrange (i.e. no added or removed capacitance). With AutoTune is disabled, **ATV** indicates the value the M800 would have tuned to if AutoTune had been enabled, not the actual added/removed capacitance which is zero.
- To reenable AutoTune, a reader writes the **A** bit to 0_b.

Refer to Table 13 for example values to configure bits in Reserved memory.

Table 15: Impinj AutoTune Value

ATV Value	Change in Input Capacitance (fF)
0_h	–100
1_h	–40
2_h	0
3_h	+40
4_h	+100

4.9 EPC Memory

In accordance with Gen2V2, M800 EPC memory contains a 16-bit CRC (StoredCRC) at memory 00_h – $0F_h$, 16 stored protocol-control (StoredPC) bits at memory 10_h – $1F_h$ and an EPC beginning at 20_h.

4.9.1 StoredCRC

At powerup, an M800 computes its StoredCRC over the StoredPC and EPC specified by the **L** bits in the StoredPC and stores the result in memory. An M800 performs this computation at every powerup.

4.9.2 StoredPC

The StoredPC comprises five programmable EPC length (**L**) bits, a read-only user memory indicator (**UMI**) bit, a read-only extended protocol control word (**XPC_W1**) indicator (XI) bit, a programmable numbering system identifier toggle (**T**) bit and eight programmable memory bits that are either Reserved for Future Use (RFU) if **T**=0 or writeable with an Application Family Identifier (AFI) if **T**=1.

- For M830 chips, **UMI** = 0_b indicates no User memory. The factory default StoredPC = 3000_h.
- For M850 chips, **UMI** = 1_b indicates User memory. The factory default StoredPC = 3400_h.

M830 and M850 do not implement **XPC_W1**.

Table 16: StoredPC Bit Values

EPC Memory Bank Bit Address	Name	How Set?	Descriptor	Setting
10_h – 14_h	**L**	Written	EPC length field	Default **L** = 00110_b
15_h	**UMI**	Fixed	User memory indicator (File_0 indicator)	0: M830 1: M850
16_h	**XI**	Fixed	XPC_W1 indicator	0: M830/M850 have no XPC_W1
17_h	**T**	Written	Numbering System Identifier Toggle	0: Tag is used in a GS1 EPCglobal™ Application 1: Tag is used in a non-GS1 EPCglobal™ Application
18_h – $1F_h$	**RFU** or **AFI**	Per the Application	Reserved for Future Use or Application Family Identifier	GS1 EPCglobal™ Application: RFU and fixed at zero Non-GS1 EPCglobal™ Application: See ISO/IEC 15961

For more details about the StoredPC or the StoredCRC, see the Gen2V2 protocol.

During an inventory round, an M800's reply to an *ACK* is determined by the StoredPC and whether the chip is truncating its EPC. Table 17 shows possible tag responses for M800 chips, following Gen2V2.

Table 17: M800 reply to an ACK command (see also the Gen2V2 protocol)

T	Truncation	M800 Reply			
		PC	XPC	EPC[1]	CRC
0	0	StoredPC(10_h–$1F_h$)	None	Full	PacketCRC
0	1	00000_b	None	Truncated	PacketCRC
1	1	00000_b	None	Truncated	PacketCRC
1	0	StoredPC(10_h–$1F_h$)	None	Full	PacketCRC

[1] Full means an EPC whose length is specified by the **L** bits in the StoredPC; truncated means an EPC whose length is shortened by a prior *Select* command specifying truncation. See *Select* command details in the Gen2V2 protocol for more information.

4.9.3 EPC

An M830 supports a maximum EPC of 128 bits; an M850 supports a maximum EPC of 96 bits (see Table 1). The default **L** bits specify a 96-bit EPC for both the M830 and M850. A reader may overwrite the **L** bits for different EPC lengths. The factory default EPC value is shown below in Table 18. The "X" nibbles in the default EPC are preserialized values that follow Impinj's Self-Serialization formula for M800 tag chips.

For more details on the pre-serialization formula used to generate the factory-programmed EPC, refer to the reference document TID Memory Maps for Monza Self-Serialization.

Table 18: Factory-Programmed EPC

Impinj Part Number	Tag Chip	Factory default StoredPC (hex)	Factory- Preprogrammed EPC (hex)
IPJ-M830A-A00	M830	3000	E280 11B0 A5XX XXXX XXXX XXXX
IPJ-M850A-A00	M850	3400	E280 11B0 A5XX XXXX XXXX XXXX

4.10 Tag Identification (TID) Memory

TID memory contains the Impinj-specific data shown in Table 19.

- 00_h-07_h are the EPCglobal™ Class ID ($E2_h$)
- 08_h is the XTID (**X**) indicator bit. **X** = 1_b indicates M830 / M850 support an extended TID, comprising a 16-bit header and 48-bit serialization.
- 09_h is the Security (**S**) indicator bit. **S** = 0_b indicates M830 / M850 do not support the *Authenticate* and/or *Challenge* commands.
- $0A_h$ is the File (F**)** indicator bit. **F** = 0_b indicates M830 / M850 do not support the *FileOpen* command.
- $0B_h$-13_h are a GS1-assigned 9-bit Mask-Designer Identifier (MDID), which for Impinj is 000000001_b. (Note: The MDID location is shown in Table 11 and Table 12; the bit details are in Table 19.)
- 14_h-$1F_h$ are the M800 series model number. See Table 20 for details on M800 model numbers.

Table 19: TID Memory Details

Memory Bank Number	Memory Bank Name	Memory Bank Bit Address	Bit Address															
			0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
10_b	TID (ROM)	80_h-$8F_h$	RFU															
		50_h-$5F_h$	TID_SERIAL [15:0]															
		40_h-$4F_h$	TID_SERIAL [31:16]															
		30_h-$3F_h$	TID_SERIAL [47:32]															
		20_h-$2F_h$	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
		10_h-$1F_h$	MDID [3:0]				Tag Model Number											
			0	0	0	1												
		00_h-$0F_h$	EPCglobal™ Class ID								X	S	F	MDID [8:4]				
			1	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0

Table 20: Impinj M800 Series Tag Model Numbers

Tag chip model	Tag Model Number	
	Hex	Binary
M830	1B0	0001 1011 0000
M850	1B0	0001 1011 0000

4.11 User Memory

An M850 has 32 bits of user memory starting at memory address 00_h. An M830 has no user memory. For further details about writing to user memory, refer to the Gen2V2 protocol.

5 ABSOLUTE MAXIMUM RATINGS

Exceeding the absolute maximum ratings listed in this section 5, or exposing an M800 to these absolute maximum ratings for extended periods, may permanently damage the chip. Operating an M800 tag chip at these absolute maximum ratings or any conditions beyond those indicated in the operational sections of this datasheet is not recommended and may compromise chip reliability.

5.1 Temperature

M800 tag chips are designed to be used within the temperature ranges listed in Table 21. These ranges specify the chip's operating, storage and survival conditions. Unless specified otherwise, an M800 will meet its functional and performance requirements when used in the operating temperature range.

Table 21: Temperature Parameters

Parameter	Min	Typ	Max	Units	Comments
Operating Temperature	–40		+85	C	Default for all functional and performance requirements except memory writes, which are limited to the Gen2V2 maximum extended temperature of 65 C.
Storage Temperature	–40		+85 +125	C	Data retention is 10 years at 85 C; one year at 125 C
Survival Temperature			+260	C	Applied for no more than one minute during chip-to-antenna assembly
Temperature Rate of Change			+/–4	C / sec	During operation

5.2 Electrostatic Discharge (ESD) Tolerance

M800 tag chips are guaranteed to survive the ESD specified in Table 22.

Table 22: ESD Limits

Parameter	Max	Units	Comments
ESD	2,000	V	HBM (Human Body Model)

5.3 NVM Use Model

M800 series tag chip memory is designed to endure 10,000 write cycles or retain data for 10 years.

6 ORDERING INFORMATION

Contact sales@impinj.com for ordering support.

Table 23: Ordering Information

Part Number	Form	Product	Processing Flow
IPJ-M830A-A00	Wafer	M830 tag chip	Padded, thinned (to ~120 µm) and diced
IPJ-M850A-A00	Wafer	M850 tag chip	Padded, thinned (to ~120 µm) and diced

7 NOTICES