Datasheet

# IMPINJ E910, E710, E510, AND E310 RAIN RFID READER CHIPS

## DATASHEET

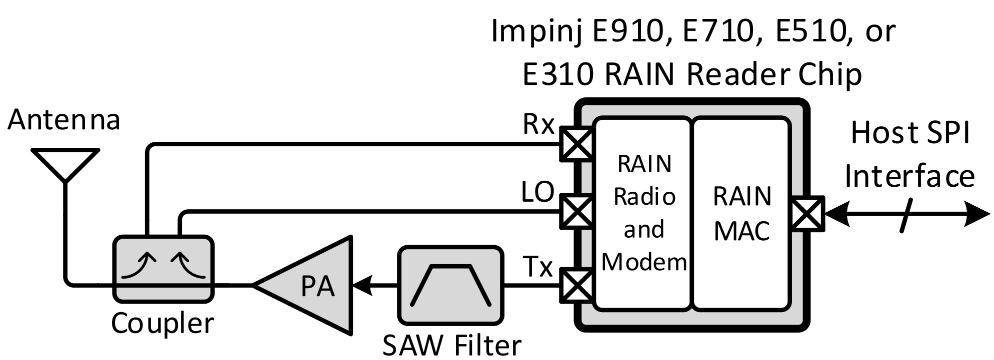
# OVERVIEW

This document constitutes the electrical, mechanical, and thermal specifications for the Impinj® E910, E710, E510, and E310 RAIN RFID reader chips. It contains a functional overview, mechanical characteristics, package signal locations, and targeted electrical specifications. An overview of the capabilities of the reader chips are shown in Table 1, and a reader system block diagram is shown in Figure 1.

**Table 1: Impinj E910, E710, E510, and E310 Reader Chips Overview**

| Specification | Description |
|---|---|
| **Air Interface Protocol** | • EPCglobal® UHF Class 1 Gen 2 / ISO 18000-63 RFID<br>• Supports Impinj Gen2X – an enhancement to the RAIN radio standard<br>• DSB-ASK, PR-ASK transmit modulation modes<br>• Dense reader mode (DRM) supported |
| **Chip Transmit Output Power** | Configurable up to +11 dBm. (External power amplifiers supported for high performance applications, up to 33 dBm total Tx Power) |
| **Chip Receive Sensitivity** | • Impinj E910: -103 dBm<br>• Impinj E710: -98 dBm<br>• Impinj E510: -93 dBm<br>• Impinj E310: -84.5 dBm<br>Note: All values in most sensitive Gen2 reader mode (20 µs TARI, 160 kHz BLF, Miller-8) at 10% PER in the "Ideal" antenna emulation configuration (described in Table 13) at the chip Rx pin<br>Sensitivity is improved by 3-5 dB across all SKUs when operating Impinj Gen2X inventory rounds |
| **Tag Read Rates** | • 1000+ tags per second<br>Note: Impinj E910 or E710, in FCC fastest RF mode, FW v1.1+. See Table 10 for details. |
| **Operating Frequencies** | 860 - 930 MHz |
| **Supported Regions** | All worldwide regions supported, including:<br>• US, Canada, and other regions following US FCC 47 CFR Ch. 1 Part 15<br>• Europe and other regions following ETSI EN 302 208-1 (v3.3.1)<br>• China, Japan, and other worldwide regions |
| **Integration** | RAIN Radio, Modem, MAC, RF Baluns, and Power Detectors included |
| **Power** | Low power consumption: (configuration dependent)<br>• Active: 550 to 1000 mW<br>• Idle: 28 to 55 mW<br>• Disabled: 0.1 to 0.5 mW |
| **Package** | 56-pin 6 mm x 6 mm sawn QFN, 0.85 mm thickness, 0.35 mm pitch |

**Figure 1 – Impinj Reader Chip-Based Circuit Block Diagram**



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# 1 INTRODUCTION

The Impinj E Family, consisting of Impinj E910, E710, E510, and E310 RAIN reader chips, provides a comprehensive portfolio of highly integrated systems-on-chips spanning a range of performance and price points. The E Family reader chips enable device OEMs to design a wide range of smart edge devices with embedded RAIN read/write capability. The reader chips deliver exceptional readability, inventory speed, range, decluttering, and data and privacy protection for identifying, locating, and authenticating next-generation, universal RAIN tags.

The E Family reader chips are designed for the RAIN radio standard (EPC Gen2 / ISO18000-63). They also support Impinj Gen2X™, an enhancement to the RAIN standard's radio and logical layers that can speed inventory, increase tag read range, declutter the environment, protect consumers, inhibit label and item counterfeiting, and reduce solution cost. Gen2X interoperates seamlessly with Gen2 / ISO 18000-63.

With 50% lower chip power consumption than the previous generation Impinj Indy series, the E Family reader chips support the design requirements for battery-powered, energy-efficient IoT devices embedding RAIN read/write capability. Additionally, the highly integrated E Family reader chips enable up to 80% smaller RAIN system designs than the Impinj Indy family, making them ideal for small, next-generation IoT devices. The E Family reader chips are also software- and pin-compatible, enabling easy performance upgrades and design reuse across various IoT devices. A broad portfolio of pre-certified modules available from the Impinj Partner Network reduces development complexity and accelerates the timeline of product development for next-generation IoT devices with RAIN read/write capability.

## 1.1 Impinj E Family Features Summary

E Family reader chips are highly integrated systems-on-chips containing all the RF and baseband blocks to interrogate and receive data from compatible RAIN tags, and an integrated microcontroller with embedded RAIN firmware providing the GS1 UHF Gen2 RAIN protocol as a pre-integrated feature. The reader chips implement direct conversion receiver architecture and operate in the worldwide UHF industrial, science, and medical (ISM) band.

E Family reader chips are a key element of the Impinj platform, a foundation for RAIN solutions. They support Impinj Gen2X Performance™ enhancements that improve reader sensitivity, increase inventory speed, improve tag power delivery, declutter tag populations, and reliably filter those populations while reducing cost. E Family reader chips also support Impinj Gen2X Protection™ enhancements that protect tag data, authenticate tag chips, and protect consumer privacy.

### 1.1.1 Impinj E Family Systems-on-Chips Integration Features

- Modem architecture uses modern digital signal processing
- Self-jammer cancellation (SJC) technology
- Fully integrated voltage-controlled oscillator (VCO) with worldwide RAIN coverage
- Integrated Power Amplifier (PA) and baluns
- High compression point quadrature down-converting mixer
- Integrated radio-frequency (RF) power detectors for forward- and reverse-power sensing
- Integrated Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs)
- Configurable digital baseband
- Integrated ARM Cortex-M0+ microcontroller core with embedded firmware
- Host Serial Peripheral Interface (SPI) clocked at up to 4 MHz
- Impinj reader chip SDK including host library source code in C and code examples in C and python

### 1.1.2 Impinj E Family Gen2X Performance Enhancements

E Family reader chips operate seamlessly in Gen2 or Gen2X inventory rounds using the reader modes described further in Section 2.4.4. Gen2X improves tag readability, especially for small tags on densely packed items. In mixed tag populations, E Family-based readers alternate Gen2 and Gen2X inventory rounds to read all tags. Regardless of the population mix, Gen2X consistently improves solution performance. When operating in Gen2X inventory rounds, the E Family reader chips boast improved:

- **Receive sensitivity**: Improved Gen2X preamble, backscatter modulation, pilot tone, and symbol encoding improve receive sensitivity across all E Family SKUs by 3 - 5 dB.
- **Inventory speed:** Configurable Gen2X RN16 parameters accelerate inventory by reducing ACK data and erroneous ACKs. Impinj TagFocus™, available in both Gen2 and Gen2X inventory rounds, allows a reader to reduce re-inventory time and focus on new tags.
- **Power delivery:** Powerup waveform shaping and extended Tari values allow E Family-based readers to deliver more power to tags, improving tag sensitivity up to 2 dB in both Gen2 and Gen2X inventory rounds.
- **Tag decluttering:** Session-dependent Gen2X RN16 protection allows E Family-based readers to discriminate which reader a tag's response is intended for, reducing cross-reads in multi-reader environments. Session-flag Booleans, available in both Gen2 and Gen2X inventory rounds, provide E Family-based readers with advanced tag decluttering techniques.
- **Tag filtering:** Tag selection during Gen2X inventory-round initiation ensures only tags-of-interest participate. Configurable Gen2X inventory responses (TID or EPC) allow TID-based solutions.

Full support for these Gen2X Performance enhancements is available with Impinj Reader Chip SDK+FW version 2.1 or later. This document includes some details on Gen2X Performance but does not detail the entirety of how to make use of these enhancements. For more information on utilizing Gen2X Performance, please request support through the Impinj Support Portal at support.impinj.com.

### 1.1.3 Impinj E Family Gen2X Protection Enhancements

E Family reader chips support Gen2X protection features to protect tag data, enable authentication, and protect consumer privacy. These protection features are part of Gen2X Protection but are also available during Gen2 inventory rounds.

- **Protecting tag data:** The E Family reader chips include support for Impinj Integra™ memory integrity checks for supporting tag chips that prevent tags sending a corrupted EPC, as well as a reader command that validates the data stored in memory on supporting tag chips.
- **Authenticating tag chips:** The E Family reader chips include support for dynamic, ISO 29167-11 authentication that, together with the Impinj Authentication Service, enables cryptographic authentication of supporting tag chips. Support for Impinj FastID™ enables rapid EPC+TID inventory and EPC ⬄ TID verification (Gen2 only). Support for Impinj Protected Mode™ (PIN-protected reversible kill) inhibits fraudulent product returns.
- **Protecting privacy:** E Family reader chips support Protected Mode. Protected Mode protects consumer privacy by configuring a supporting tag to be nonresponsive to a reader unless the reader first provides a correct PIN. Support for short-range mode reduces tag read range by roughly 10 times (20 dB).

Full support for these Gen2X Protection enhancements is available with Impinj Reader Chip SDK+FW version 2.0 or later. This document includes some details on Gen2X Protection but does not detail the entirety of how to make use of these enhancements. For more information on utilizing Gen2X Protection, please request support through the Impinj Support Portal at support.impinj.com.

## 1.2 Reference Documents

The conventions used in the UHF Gen2 Specification (normative references, terms and definitions, symbols, abbreviated terms, and notation) were adopted in the drafting of this datasheet. Users of this datasheet should familiarize themselves with the UHF Gen2 Specification.

The Impinj E Family reader chips are fully compliant with the protocol specifications and local regulation documents in Table 2:

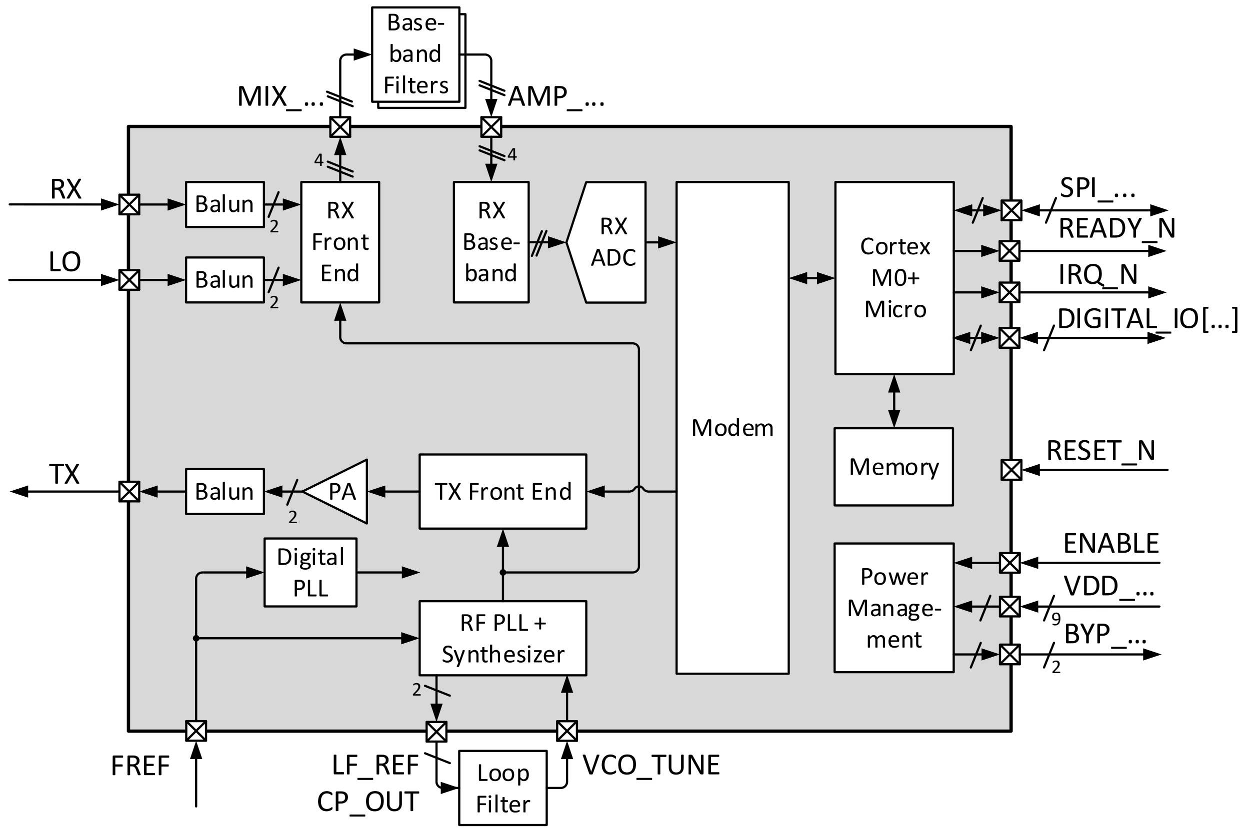
**Table 2: Specification Documents**

| Protocol Specification Documents | Local Regulation Documents |
|---|---|
| • GS1 EPCGlobal Interoperability Test System for EPC compliant Class-1 Gen-2 UHF RFID | • FCC 47 CFR Ch. 1, part 15<br>• ETSI EN 302 208-1 v2.1.1 |

## 1.3 Block Diagram

Figure 2 contains a detailed internal block diagram of the Impinj E Family reader chips. The architecture is based on direct conversion for both the transmitter and receiver.

**Figure 2 – Impinj Reader Chip Detailed Internal Block Diagram**

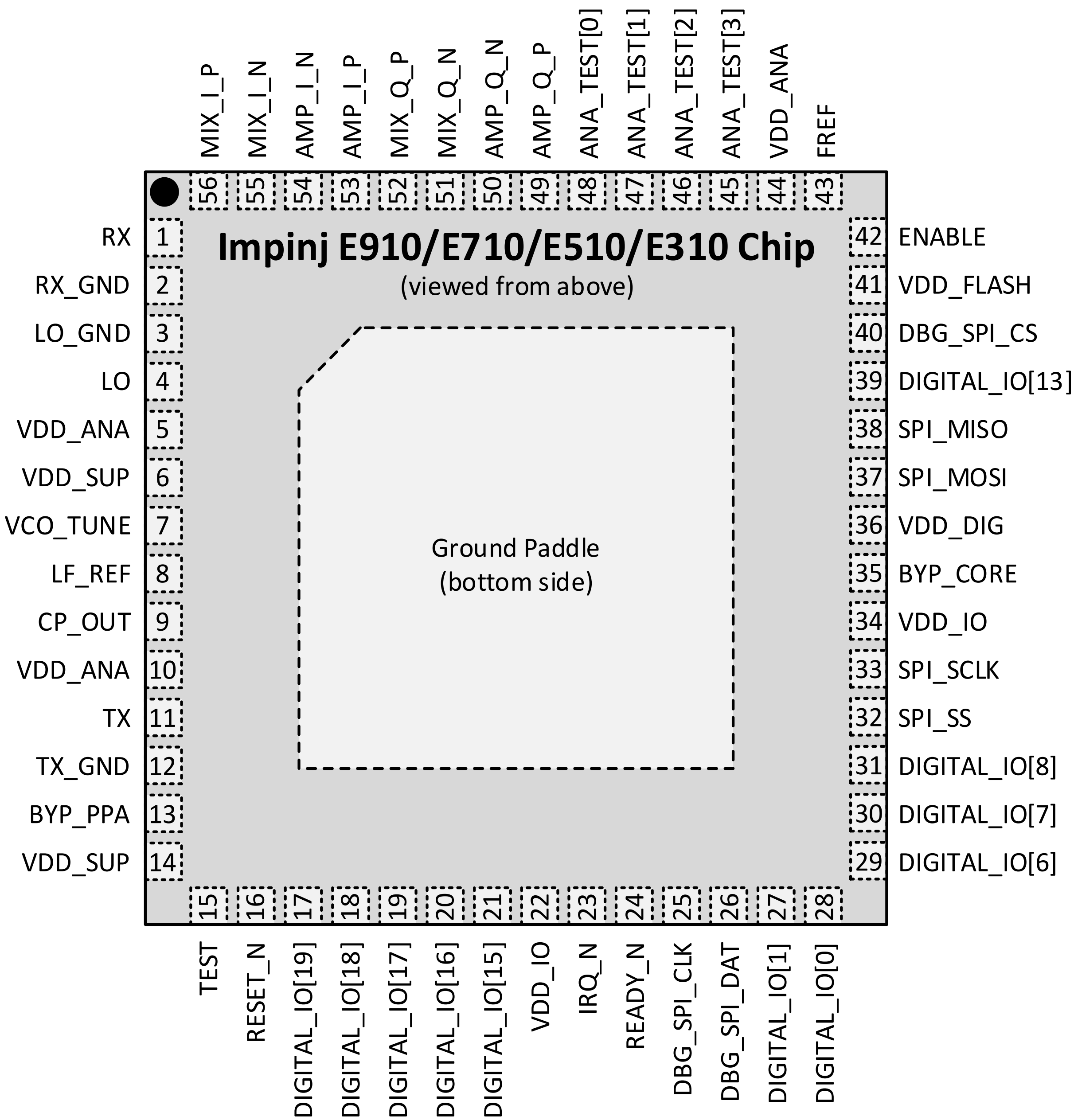


# 2 SPECIFICATIONS

## 2.1 Pin Listing and Signal Definitions

The Impinj E Family reader chips are offered in a 56-pin 6x6 mm QFN package. They require an external SAW filter and directional coupler in most configurations to implement a full radio circuit, along with a power amplifier (PA) if higher transmit power is required. The pinout for the 6x6 mm QFN is shown graphically in Figure 3 and in a list in Table 3. For package dimensions, see section 7.1 - Package Dimensions.

**Figure 3 – Impinj E Family Reader Chip Pinout**




**Note:** Diagram not to scale

**Table 3: Impinj E Family Reader Chip Pin Signal Listing**

| Pin # | Pin Name | Type | Description |
|---|---|---|---|
| 1 | RX | RF In | RFID receive signal |
| 2 | RX_GND | RF Ground | RFID receive signal ground |
| 3 | LO_GND | RF Ground | RFID local oscillator/self-jammer cancellation reference signal ground |
| 4 | LO | RF In | RFID local oscillator/self-jammer cancellation reference signal |
| 5 | VDD_ANA | Power Supply | Analog power supply |
| 6 | VDD_SUP | Power Supply | Supervisory power supply |
| 7 | VCO_TUNE | Analog Input | VCO tuning input |
| 8 | LF_REF | Analog Output | PLL loop filter reference |
| 9 | CP_OUT | Analog Output | PLL charge pump output |
| 10 | VDD_ANA | Power Supply | Analog power supply |
| 11 | TX | RF Out | RFID transmit signal |
| 12 | TX_GND | RF Ground | RFID transmit signal ground |
| 13 | BYP_PPA | Power Bypass | Power amplifier power supply bypass |
| 14 | VDD_SUP | Power Supply | Supervisory power supply |
| 15 | TEST | DNU | Reserved for Impinj usage. Should be tied to ground. |
| 16 | RESET_N | Digital Input | Chip reset signal (active low) |
| 17 | DIGITAL_IO[19] | Digital IO | Digital input/output |
| 18 | DIGITAL_IO[18] | Digital IO | Digital input/output |
| 19 | DIGITAL_IO[17] | Digital IO | Digital input/output |
| 20 | DIGITAL_IO[16] | Digital IO | Digital input/output |
| 21 | DIGITAL_IO[15] | Digital IO | Digital input/output |
| 22 | VDD_IO | Power Supply | Digital input/output power supply |
| 23 | IRQ_N | Digital Output | Interrupt signal output (active low) |
| 24 | READY_N | Digital IO | Host SPI interface slave ready signal output (active low), boot to application/bootloader pin |
| 25 | DBG_SPI_CLK | Digital Output | Debug SPI interface master clock (SPI out for FW troubleshooting) |
| 26 | DBG_SPI_DAT | Digital Output | Debug SPI interface master MOSI (SPI out for FW troubleshooting) |
| 27 | DIGITAL_IO[1] | Digital IO | Digital input/output |
| 28 | DIGITAL_IO[0] | Digital IO | Digital input/output |
| 29 | STARTUP / DIGITAL_IO[6] | Digital IO | Digital input/output (must be pulled or driven high at startup) |
| 30 | DIGITAL_IO[7] | Digital IO | Digital input/output |
| 31 | DIGITAL_IO[8] | Digital IO | Digital input/output |
| 32 | SPI_SS | Digital Input | Host SPI interface slave select (active low) |
| 33 | SPI_SCLK | Digital Input | Host SPI interface clock |
| 34 | VDD_IO | Power Supply | Input/output power supply |
| 35 | BYP_CORE | Power Bypass | Core power supply bypass |
| 36 | VDD_DIG | Power Supply | Digital power supply |
| 37 | SPI_MOSI | Digital Input | Host SPI interface master output slave input |
| 38 | SPI_MISO | Digital Output | Host SPI interface master input slave output |

| Pin # | Pin Name | Type | Description |
|---|---|---|---|
| **39** | DIGITAL_IO[13] | Digital IO | Digital input/output |
| **40** | DBG_SPI_CS | Digital Output | Debug SPI interface master chip select (SPI out for FW troubleshooting) |
| **41** | VDD_FLASH | Power Supply | Flash memory power supply |
| **42** | ENABLE | Digital Input | Chip enable input |
| **43** | FREF | Clock Input | 24 MHz PLL reference clock signal |
| **44** | VDD_ANA | Power Supply | Analog power supply |
| **45** | ANA_TEST[3] | Analog IO | Analog test signal |
| **46** | ANA_TEST[2] | Analog IO | Analog test signal |
| **47** | ANA_TEST[1] | Analog IO | Analog test signal |
| **48** | ANA_TEST[0] | Analog IO | Analog test signal |
| **49** | AMP_Q_P | Analog Input | Q post-mixer amplifier quadrature differential input (positive) |
| **50** | AMP_Q_N | Analog Input | Q post-mixer amplifier quadrature differential input (negative) |
| **51** | MIX_Q_N | Analog Output | Q mixer quadrature differential output (negative) |
| **52** | MIX_Q_P | Analog Output | Q mixer quadrature differential output (positive) |
| **53** | AMP_I_P | Analog Input | I post-mixer amplifier quadrature differential input (positive) |
| **54** | AMP_I_N | Analog Input | I post-mixer amplifier quadrature differential input (negative) |
| **55** | MIX_I_N | Analog Output | I mixer quadrature differential output (negative) |
| **56** | MIX_I_P | Analog Output | I mixer quadrature differential output (positive) |
| **Paddle** | GND | GND | Chip ground |

## 2.2 IO Connections and Configurations

The Impinj E Family reader chips have input and output pins that are used to configure the devices. A host device such as an MCU or an application processor can control and monitor these pins. This section enumerates the required, recommended, and optional connections, and gives notes on their states.

**Note:** Impinj E Family reader chip firmware versions 2.1 and earlier don't support using the DIGITAL_IO pins as inputs. This feature may be added in a future firmware release.

### 2.2.1 Digital IO Default Drive Modes

The Impinj E Family reader chip digital IOs start up in either a pull-up or pull-down drive mode. The DIGITAL_IOs can be reconfigured using the reader chip firmware operations, but at startup, their drive modes will be as shown in Table 4. The IO pull-up and pull-down resistance is specified in Table 25.

**Table 4: Impinj E Family Reader Chip Digital IO Default Drive Modes**

| Pin # | Pin Name | Type | Default Drive Mode |
|---|---|---|---|
| **15** | TEST | DNU | Pull-down |
| **16** | RESET_N | Digital Input | Pull-up |
| **17** | DIGITAL_IO[19] | Digital IO | Pull-up |
| **18** | DIGITAL_IO[18] | Digital IO | Pull-up |
| **19** | DIGITAL_IO[17] | Digital IO | Pull-up |
| **20** | DIGITAL_IO[16] | Digital IO | Pull-up |
| **21** | DIGITAL_IO[15] | Digital IO | Pull-up |
| **27** | DIGITAL_IO[1] | Digital IO | Pull-up |
| **28** | DIGITAL_IO[0] | Digital IO | Pull-up |

| Pin # | Pin Name | Type | Default Drive Mode |
|---|---|---|---|
| **29** | STARTUP / DIGITAL_IO[6] | Digital IO | Pull-up |
| **30** | DIGITAL_IO[7] | Digital IO | Pull-up |
| **31** | DIGITAL_IO[8] | Digital IO | Pull-up |
| **39** | DIGITAL_IO[13] | Digital IO | Pull-up |

### 2.2.2 Host IO Connections

**Table 5: Impinj E Family Reader Chip Host Device Connections**

| Category | Pin Name | Type | Connection | Notes |
|---|---|---|---|---|
| **SPI (Serial Peripheral Interface)** | SPI_SS | Digital Input | Required | SPI slave select (active low)<br>Required for SPI communication with the host. |
| | SPI_SCLK | Digital Input | Required | SPI clock<br>Required for SPI communication with the host. |
| | SPI_MOSI | Digital Input | Required | SPI master output slave input<br>Required for SPI communication with the host. |
| | SPI_MISO | Digital Output | Required | SPI master input slave output<br>Required for SPI communication with the host. |
| | READY_N | Digital IO | Required | SPI slave ready signal output (active low), startup boot to application/bootloader pin<br>Required for SPI communication with the host. |
| **Reader Chip Control** | ENABLE | Digital Input | Required | Chip enable input<br>Allows host to control startup and put chip in a low power mode. Details on control below. |
| | RESET_N | Digital Input | Required | Chip reset signal (active low)<br>Allows host to reset the reader chip without cycling the power. Must be sequenced as described in the next section.<br>The reader chip drives this signal strong low during startup, so it must not be driven strong high externally. |
| **Firmware State** | IRQ_N | Digital Output | Recommended | Interrupt signal output (active low)<br>Indicates to the host when data is ready on the reader chip. Can be left unconnected if host queries the reader chip regularly. |

### 2.2.3 IO conditions

Certain Impinj E Family reader chip IOs must be in a specific electrical state for specific optional or mandatory operational states. They are listed below. These are in addition to the power supply pins, synthesizer pins, RF and baseband interface pins, etc. More details on startup sequence timing are shown in section 2.3.1 - Power Up Sequence.

ENABLE must be driven high to enable the reader chip. It should only be driven high after a stable 24 MHz clock signal is present at the FREF pin. ENABLE may be driven low to put the part into "Shutdown" mode, as described in section 3.7 - Power Modes.

RESET_N must be allowed to be driven low by the reader chip entering startup. If it is driven low to reset the part, it must be released >500 µs after the ENABLE pin is driven high. An internal pull-up resistor will pull the pin high. RESET_N may be used to reset the reader chips during operation.

DIGITAL_IO[6] must be driven high during reader chip firmware startup (after the RESET_N pin goes high, and before the READY_N pin goes low). This may be accomplished either by controlling the DIGITAL_IO[6] pin using a host device, or by applying a strong high or pullup voltage to the pin. If a pullup is applied, the pin can be reconfigured as a strong drive by the reader chip and used to drive an external signal after startup is complete. On the Impinj E710 development board, this pin is pulled high with a 10 kΩ resistor.

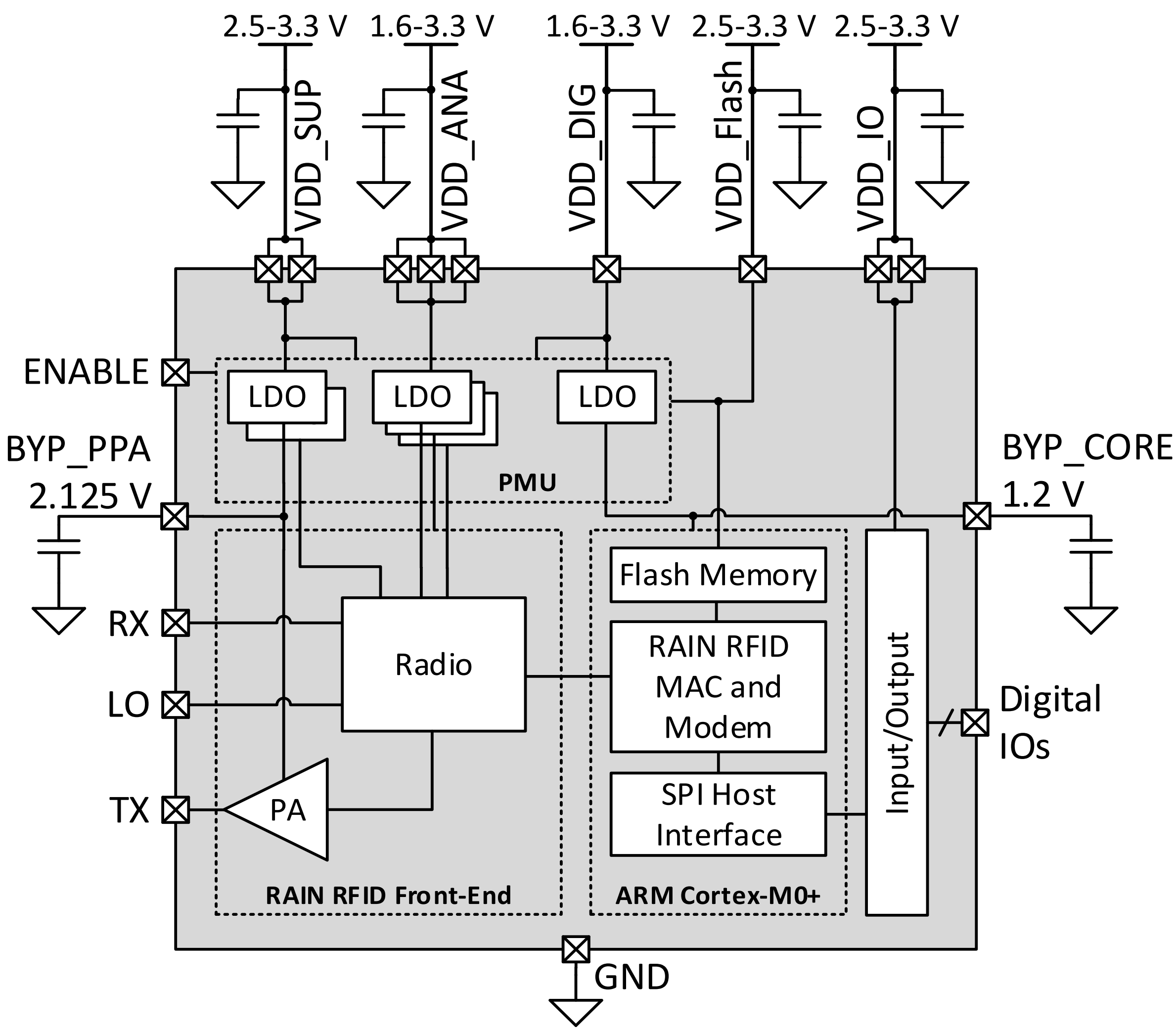
 

READY_N must be driven strong low for 8706 FREF clock cycles (~362.75 µs) at startup (after the ENABLE pin goes high) to force the reader chip into bootloader mode. After a normal startup to application (not to bootloader) the READY_N pin will be driven low by E710 to indicate that startup has completed, and the reader chip is ready to communicate with the host via the SPI. Interface. The READY_N pin is also part of the SPI signaling wireline, as described in section 4.2 - SPI Digital Communication Interface.

## 2.3 Power Supply

The Impinj E Family reader chips have multiple power supply pins, and to achieve maximum performance, they must be properly configured. A block diagram of the reader chip's power supplies, their ranges, and the circuits they drive is shown in Figure 4.

**Figure 4 – Impinj E Family Reader Chip Power Supply Block Diagram**




VDD_SUP, VDD_IO, and VDD_FLASH must all be powered at the same voltage, within the range of 2.5 to 3.3 volts. VDD_ANA and VDD_DIG must be powered at the same voltage, within the range of 1.6 to 3.3 volts, and lower than or equal to the VDD_SUP voltage. Note that these values are nominal, and the actual maximum and minimum values have additional margin, as shown in Table 7.

All the supplies may share the same voltage, as long as it is within the shared range of 2.5 to 3.3 volts. Power consumption is optimized when each of the supplies are at their lowest allowed voltage (e.g. 1.6 volts for VDD_ANA and VDD_DIG, and 2.5 volts for VDD_SUP, VDD_IO, and VDD_FLASH). The valid range of supply voltage combinations is shown in Figure 5, and examples of both minimal power dual supply and a 3.3 V single supply are shown in Figure 6. Ferrite beads are used for isolation of the power supplies. These diagrams are simplifications, and both passive and active isolation of the power supplies can improve performance. See the Impinj E710 Development Board Application Note for more details.

**Figure 5 – Impinj E Family Reader Chip Valid Power Supply Voltage Conditions**

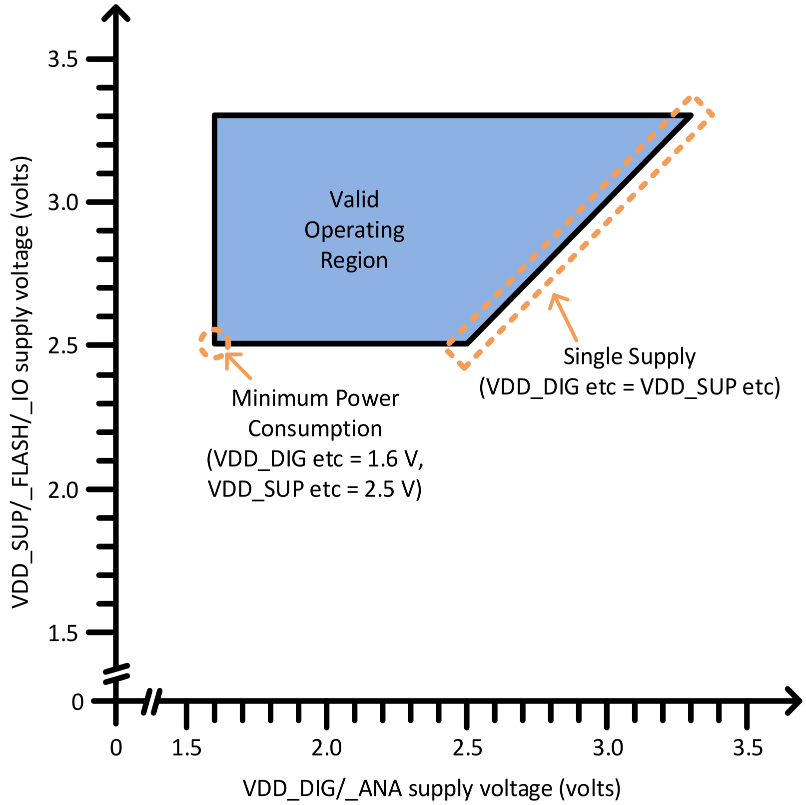
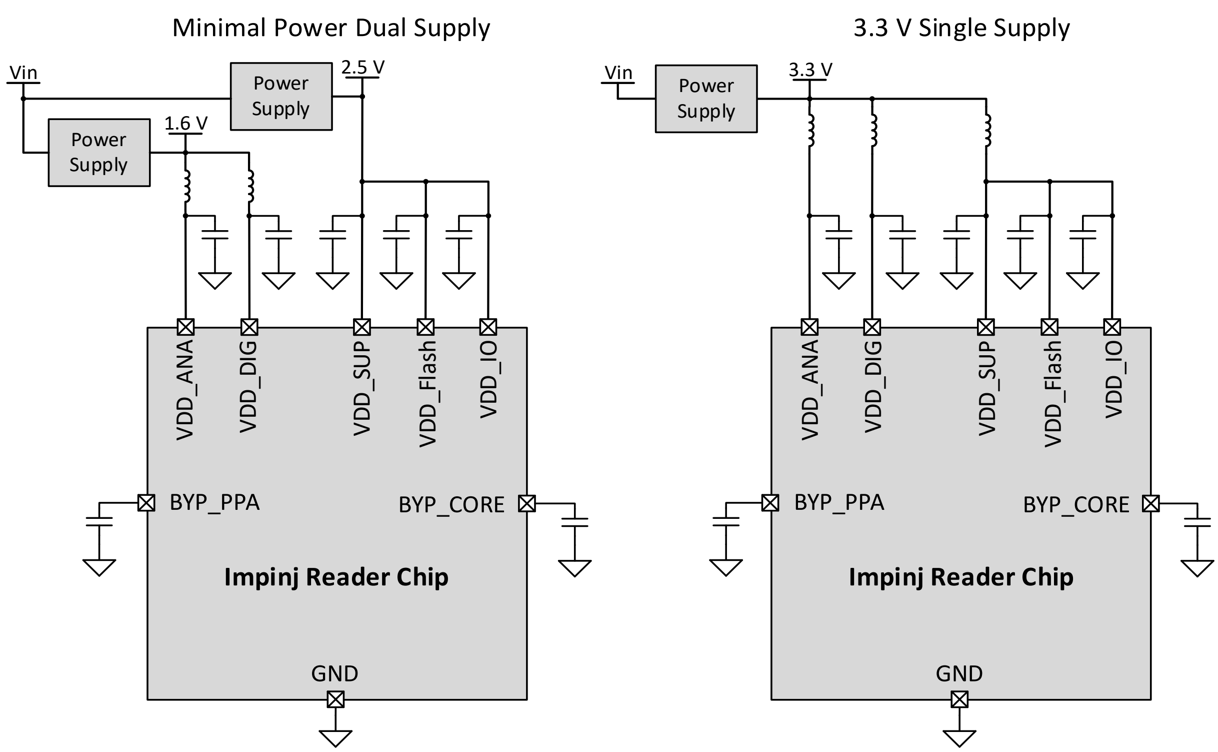



**Figure 6 – Impinj E Family Reader Chip Example Power Supply Configurations**



The supply pins must be bypassed with external bypass capacitors, which will also filter power supply noise. See the Impinj E710 Development Board Application Note for an example implementation. The individual bypass capacitors should be placed close to the pins that they are bypassing. When an array of bypass capacitors is shown on the same net connecting multiple power pins, the array should be split up physically such that each pin has its own bypass capacitor.

BYP_PPA and BYP_CORE are not power supply inputs, but rather external bypass pins for the internally regulated power supplies. They should be externally bypassed with capacitance, but not driven. External bypass capacitance must be 10 µF or above, as demonstrated in the Impinj E710 development board. No external loads should be placed on these supply voltages. BYP_CORE is regulated to 1.2 V nominal. BYP_PPA is regulated to 2.125 V nominal. The un-bypassed, internal only analog supply BYP_ANA is regulated to 1.2 V nominal.

All of the duplicated power supplies (e.g. pins 6 and 14, both connected to VDD_SUP, see also VDD_ANA and VDD_IO) must be connected external to the reader chip.

For more details on potential external power supply implementations, see the Impinj E710 Development Board Application Note.

### 2.3.1 Power Up Sequence

The Impinj E Family reader chips must be powered up using a specific sequence of conditions on the power supplies, IOs, and other pins. This sequence is described verbally in the paragraph below, in a numbered list format following that, and graphically in Figure 7.

The power-up sequence must start by powering the VDD_SUP, VDD_IO, and VDD_FLASH supplies. The VDD_DIG and VDD_ANA power supplies may be powered at the same time or after the VDD_SUP, VDD_IO, and VDD_FLASH supplies. To reiterate, the VDD_DIG and VDD_ANA supplies must not be powered up before the other power supplies on the device. A 24 MHz clock must be present at FREF for the part to start up successfully. The part will not startup if the ENABLE pin is not high, or if the RESET_N pin is not allowed to be driven low by the reader chip. Approximately 500 µs after the enable pin goes high, the part will release the RESET_N pin, and firmware startup will begin. DIGITAL_IO[6] must be pulled or driven strong high during firmware startup, and then may be used as a digital input or output per application requirements. The READY_N pin will be driven low by the reader chip when firmware startup has completed, and the part is ready to communicate via SPI with the host device. The READY_N pin may also be driven low when RESET_N is released during startup to force the part into the bootloader mode. For more details on this, see section 2.2.3 - IO conditions.

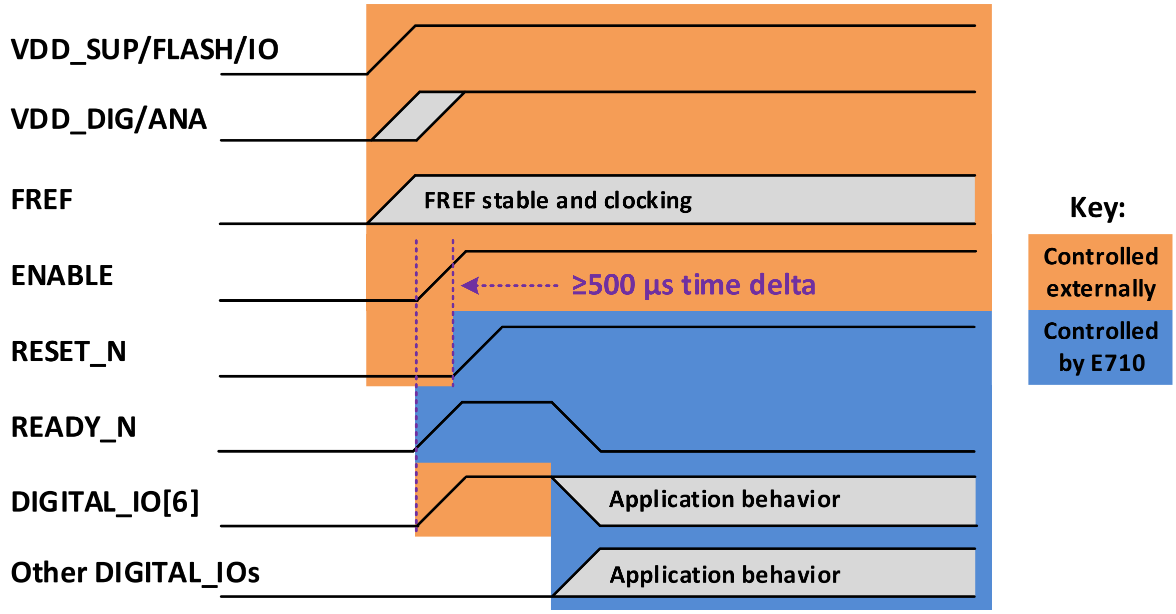
This startup sequence is implemented in the Impinj reader chip SDK, specifically in **`power_transactor.c`** API **`ex10_power_up_to_application(…)`**.

For more detail on startup, including detail on how to boot to the bootloader, see the firmware HTML documentation in the Impinj Ex10 Reader Chip SDK Specification.

1. Power the reader chip
    a. VDD_SUP, VDD_FLASH, and VDD_IO should be powered up before or simultaneously with VDD_DIG and VDD_ANA
    b. A 24 MHz clock signal should be applied to FREF simultaneously or after power is applied
2. ≥5 ms after powering the chip, apply initial IO conditions to startup the reader chip
    a. RESET_N must be driven low by the host
    b. DIGITAL_IO[6] should be pulled high by the host
    c. ENABLE should be driven high by the host
    d. All other IOs should be left floating
3. ≥10 ms after applying initial IO conditions, apply final IO conditions to startup the reader chip
    a. RESET_N should be released by the host
    b. After approximately 500 µs, the RESET_N pin will be driven high by the reader chip, and firmware startup will begin
4. Observe the conclusion of startup

a. When the READY_N pin is driven low by the reader chip, firmware startup has completed
b. At this point, the reader chip firmware will respond to SPI commands, and all the DIGITAL_IOs can be used for other purposes
c. The ENABLE pin should still be driven high, and RESET_N should be left floating during operation

**Figure 7 – Impinj E Family Reader Chip Startup Power Supply and IO Sequencing**

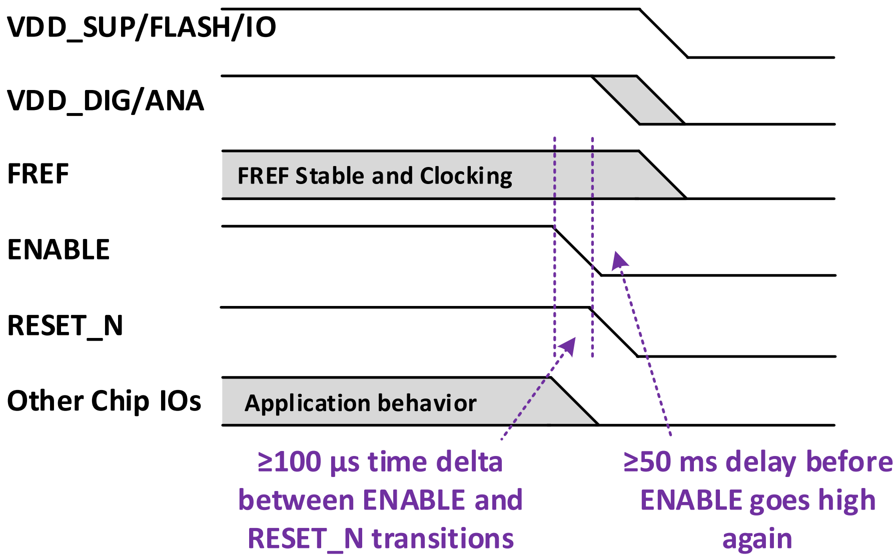



### 2.3.2 Power Down Sequence

The Impinj E Family reader chips must be powered down in a specific sequence. That sequence is described in detail below and shown in Figure 8.

1. Disable the reader chip
    a. The reader chip can be disabled by driving the ENABLE pin low
        i. At this point, the reader chip will stop responding to SPI communication, and application driven IO behaviors will cease
    b. The ENABLE pin must be driven low for 100 µs before the reader chip is reset or powered down
        i. The FREF input must continue clocking until this 100 µs delay has completed
2. Reset and power down the reader chip
    a. All chip IOs should either be left floating(high impedance) or driven to ground
    b. FREF may stop clocking
    c. The RESET_N pin may be driven low
    d. The VDD pins may be driven low, which will also drive RESET_N low if it is floating
        i. VDD_DIG and VDD_ANA should be driven low either before or simultaneously with VDD_SUP, VDD_FLASH, and VDD_DIG
3. The reader chip should be left powered down for at least 50 ms before it is powered up again

Figure 8 – Impinj E Family Reader Chip Power Down Sequence




### 2.3.3 Disable-Enable Sequence

The Impinj E Family reader chips must be disabled and re-enabled in a specific sequence. That sequence is described in detail below and shown in Figure 9.

The Disable functionality allows reduced power consumption without removing power from the reader chip. Reader designs should still maintain the ability to power down the reader chip to resolve unrecoverable states.

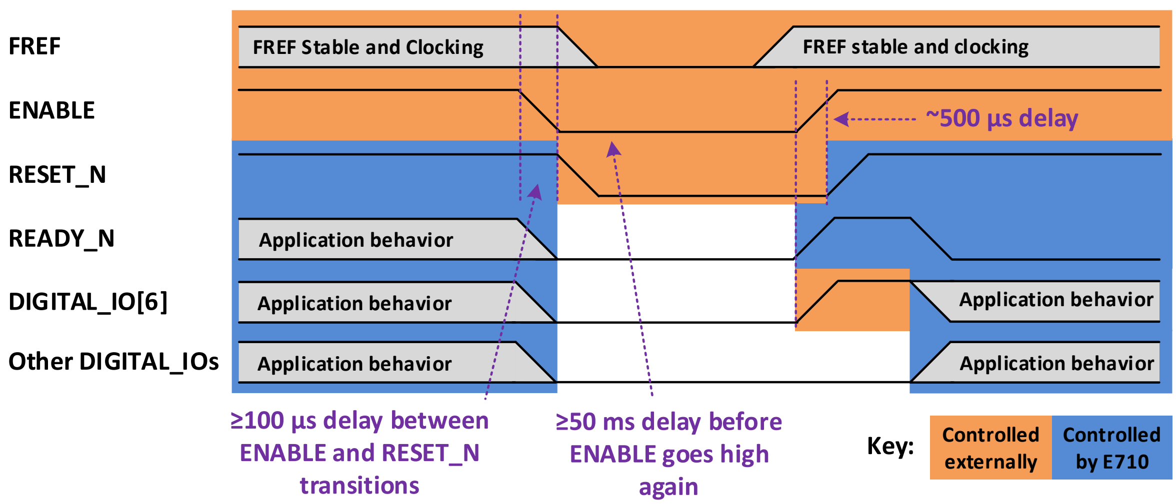
**Note:** It is critical that the ENABLE pin goes low 100 µs before RESET_N transitions low. If this condition is not met, the reader chip could enter a state that is only recoverable through a chip power cycle.

1. Drive the enable pin low
    a. The reader chip should be disabled by driving the ENABLE pin low
        i. At this point, the reader chip will stop responding to SPI communication, and application driven IO behaviors will cease
    b. The ENABLE pin must be driven low for 100 µs before the RESET_N pin is driven low
        i. The FREF input must continue clocking until this 100 µs delay has completed
2. Reset the reader chip
    a. All chip IOs should either be left floating (high impedance) or driven to ground
    b. FREF may stop clocking
    c. The RESET_N pin should be driven low
3. Chip disabled
    a. At this point, the reader chip is disabled, and will consume reduced current
    b. The reader chip must be left disabled for at least 50 ms before it is enabled again
4. After ~5 ms, Apply initial IO conditions to startup the reader chip
    a. RESET_N must be driven low by the host
    b. DIGITAL_IO[6] should be pulled high by the host
    c. ENABLE should be driven high by the host
    d. All other IOs should be left floating
5. After ~10 ms, apply final IO conditions to startup the reader chip
    a. RESET_N should be released by the host

b. After approximately 500 µs, the RESET_N pin will be driven high by the reader chip, and firmware startup will begin

6. Observe the conclusion of startup
   a. When the READY_N pin is driven low by the reader chip, firmware startup has completed
   b. At this point, the reader chip firmware will respond to SPI commands, and all of the DIGITAL_IOs can be used for other purposes
   c. The ENABLE pin should still be driven high, and RESET_N should be left floating during operation

**Figure 9 – Impinj E Family Reader Chip Disable-Enable Sequence**



## 2.4 Electrical Specifications

### 2.4.1 Absolute Maximum Ratings

The absolute maximum ratings in Table 6 define the limitations for electrical and thermal stresses. These limits prevent permanent damage to the Impinj E Family reader chips. If the reader chip is exposed to conditions outside of these ranges, it is no longer guaranteed to operate properly or meet the performance specifications listed in this document, even after conditions return to the valid ranges.

**Table 6: Absolute Minimum and Maximum Ratings**

| Parameter | Min | Max | Unit | Conditions |
|---|---|---|---|---|
| **VDD_SUP/_FLASH/_IO voltage** | -0.3 | 3.6 | volts DC | |
| **VDD_DIG/_ANA voltage** | -0.3 | 3.6 | volts DC | |
| **Chip IO applied voltage** | GND - 0.5 | VDD_IO + 0.5 | volts DC | Under typical conditions, IO voltages should not go below GND or above VDD_IO |
| **ESD, Power supply and IO pins** | N/A | N/A | N/A | HBM Class 3A |
| | N/A | N/A | N/A | CDM Class C0b |
| **ESD, RF pins** | N/A | N/A | N/A | HBM Class 2 |
| | N/A | N/A | N/A | CDM Class C0b |
| **TX, LO, RX port RF input power** | N/A | +20 | dBm | Note: Optimal RF performance achieved at lower power levels, see Table 18 |
| **Storage Temperature** | -55 | 125 | °C | |
| **Case Temperature** | N/A | 260 | °C | For reflow purposes |
| **Package Moisture Sensitivity Level** | N/A | N/A | N/A | Moisture Sensitivity Level (MSL) 3 |

### 2.4.2 Operating Conditions

The operating conditions listed in this section describe the conditions under which the Impinj E Family reader chips will operate properly and meet the performance specifications listed in this document. If these conditions are not met, the reader chip will not perform as expected, but will also not suffer permanent damage.

**Table 7: Chip Operating Conditions**

| Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|
| **VDD_SUP/_FLASH/_IO voltage** | 2.375 | 2.5 or 3.3 | 3.465 | volts DC | All supplies in this row must be operated at the same voltage<br>Typ column lists common voltages |
| **VDD_DIG/_ANA voltage** | 1.52 | 1.6, 2.5, or 3.3 | 3.465 | volts DC | All supplies in this row must be operated at the same voltage<br>VDD_DIG must be ≤ VDD_SUP<br>Typ column lists common voltages |
| **Operating Ambient Temperature** | -40 | N/A | 85 | °C | Analysis performed using worst case power consumption, the $\theta_{JA}$ PCB layout and conditions |
| **Junction Temperature** | | N/A | 125 | °C | |
| **Junction to Ambient Thermal Resistance ($\theta_{JA}$)** | | 27.8 | | °C/W | Typical 4-layer PCB layout, 9 vias below e-pad, no heat sink, no forced airflow |

### 2.4.3 Power Supply Specifications

**Table 8: Chip Power Consumption**

| Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|
| **Chip performing inventory, transmitting at +11 dBm**<br>**Note: SJC does not increase power consumption.** | N/A<br>N/A<br>N/A<br>N/A | 950<br>700<br>650<br>550 | 1065<br>800<br>750<br>650 | mW<br>mW<br>mW<br>mW | 3.3 V Single Supply<br>2.5 V Single Supply<br>3.3 / 1.6 V Dual Supply<br>2.5 / 1.6 V Dual Supply |
| **Chip idle**<br>**(chip powered with firmware executing, but without host configuration performed)** | N/A<br>N/A<br>N/A<br>N/A | 48<br>38<br>30<br>28 | 75<br>60<br>46<br>44 | mW<br>mW<br>mW<br>mW | 3.3 V Single Supply<br>2.5 V Single Supply<br>3.3 / 1.6 V Dual Supply<br>2.5 / 1.6 V Dual Supply |
| **Chip disabled** | N/A<br>N/A<br>N/A<br>N/A | 0.4<br>0.1<br>0.3<br>0.1 | 0.5<br>0.2<br>0.4<br>0.2 | mW<br>mW<br>mW<br>mW | 3.3 V Single Supply<br>2.5 V Single Supply<br>3.3 / 1.6 V Dual Supply<br>2.5 / 1.6 V Dual Supply |
| **Chip held in reset** | N/A | | 50 | mW | Using RESET_N pin |

**Table 9: Chip Typical Current Consumption Distribution**

| | VDD_ANA | VDD_DIG | VDD_FLASH | VDD_IO | VDD_SUP | Units |
|---|---|---|---|---|---|---|
| Power Supply Condition: Single Supply 3.3 V | | | | | | |
| **Supply Voltage** | 3.3 | 3.3 | 3.3 | 3.3 | 3.3 | volts |
| **Chip Active** | 133.8 | 34.3 | 0.0 | 0.1 | 115.0 | mA |
| **Chip Idle** | 0.4 | 10.2 | 0.0 | 0.1 | 3.8 | mA |
| **Chip Disabled** | 0.0 | 0.1 | 0.0 | 0.0 | 0.0 | mA |
| Power Supply Condition: Single Supply 2.5 V | | | | | | |
| **Supply Voltage** | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | volts |
| **Chip Active** | 133.0 | 33.6 | 0.0 | 0.0 | 115.3 | mA |
| **Chip Idle** | 0.4 | 10.1 | 0.0 | 1.1 | 3.6 | mA |
| **Chip Disabled** | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | mA |
| Power Supply Condition: Dual Supply 3.3 V / 1.6 V | | | | | | |
| **Supply Voltage** | 1.6 | 1.6 | 3.3 | 3.3 | 3.3 | volts |
| **Chip Active** | 133.8 | 34.3 | 0.0 | 0.1 | 115.0 | mA |
| **Chip Idle** | 0.4 | 10.2 | 0.0 | 0.1 | 3.8 | mA |
| **Chip Disabled** | 0.0 | 0.1 | 0.0 | 0.0 | 0.0 | mA |
| Power Supply Condition: Dual Supply 2.5 V / 1.6 V | | | | | | |
| **Supply Voltage** | 1.6 | 1.6 | 2.5 | 2.5 | 2.5 | volts |
| **Chip Active** | 133 | 33.6 | 0.0 | 0.0 | 115.3 | mA |
| **Chip Idle** | 0.4 | 10.1 | 0.0 | 1.1 | 3.6 | mA |
| **Chip Disabled** | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | mA |

**Note:** All values typical, rounded to the nearest tenth of a mA

### 2.4.4 Gen2 and Gen2X Reader Modes and Performance Specifications

The E Family reader chips operate seamlessly across Gen2 and Gen2X inventory rounds using the reader modes detailed in Table 10 and Table 11 below. To initiate a Gen2 inventory round, the E Family reader chips send a Gen2 preamble followed by a *Query* command, and for a Gen2X inventory round, the E Family reader chip sends a Gen2X preamble followed by a *Scan* command. The reader controls whether subsequent inventory rounds are Gen2 or Gen2X by sending a *Query* or *Scan*, respectively. Supporting tag chips share session and select flag values across Gen2 and Gen2X inventory rounds, allowing seamless tag population management across Gen2 and Gen2X.

All other commands are the same between Gen2 and Gen2X, but the frame-syncs are different. Gen2 inventory rounds use a Gen2 frame-sync whereas Gen2X inventory rounds use a Gen2X frame-sync. When in a Gen2 inventory round, tag chips ignore commands with a Gen2X frame sync, and vice versa. All commands except *Query* and *Scan* are common between Gen2 and Gen2X inventory rounds – the only difference is the frame-sync.

For more details on Gen2X inventory rounds please request support through the Impinj Support Portal at support.impinj.com.

**Table 10: RAIN Gen2 Inventory Round Reader Mode IDs and Parameters**

| FCC Mode ID | ETSI LB Mode ID | ETSI UB Mode ID | Supported Regions* | Reader Mode Optimization | Forward Link Modulation | Tari (µs) | PIE | BLF (kHz) | Back-scatter Link Modulation |
|---|---|---|---|---|---|---|---|---|---|
| **103** | N/A | N/A | FCC | FCC Read Rate | DSB-ASK | 6.25 | 1.5 | 640 | FM0 |
| **102** | N/A | **302** | ETSI UB+ | ETSI UB Read Rate | PR-ASK | 7.5 | 2.0 | 640 | FM0 |
| **120** | N/A | N/A | FCC | FCC Hybrid | DSB-ASK | 6.25 | 1.5 | 640 | Miller M=2 |
| **104** | N/A | N/A | FCC | FCC Read Rate | DSB-ASK | 6.25 | 1.5 | 320 | FM0 |
| **124** | N/A | **323** | ETSI UB+ | ETSI UB Hybrid | PR-ASK | 7.5 | 2.0 | 640 | Miller M=2 |
| N/A | **203** | N/A | Japan+ | Japan Read Rate | PR-ASK | 12.5 | 1.5 | 426 | FM0 |
| N/A | **202** | N/A | ETSI LB+ | ETSI LB Read Rate | PR-ASK | 15 | 2.0 | 426 | FM0 |
| N/A | **226** | N/A | Japan+ | Japan Hybrid | PR-ASK | 12.5 | 1.5 | 426 | Miller M=2 |
| **147** | N/A | **344** | ETSI UB+ | ETSI UB DRM | PR-ASK | 7.5 | 2.0 | 640 | Miller M=4 |
| **148** | N/A | **345** | ETSI UB+ | ETSI UB Hybrid | PR-ASK | 7.5 | 1.5 | 640 | Miller M=4 |
| N/A | **225** | N/A | ETSI LB+ | ETSI LB Hybrid | PR-ASK | 15 | 2.0 | 426 | Miller M=2 |
| N/A | **224** | N/A | Japan+ | Japan Hybrid | PR-ASK | 12.5 | 1.5 | 320 | Miller M=2 |
| **125** | **223** | **325** | ETSI LB+ | ETSI LB Hybrid | PR-ASK | 15 | 2.0 | 320 | Miller M=2 |
| **123** | **222** | **324** | ETSI LB+ | ETSI LB Hybrid | PR-ASK | 20 | 2.0 | 320 | Miller M=2 |
| **141** | **241** | **342** | ETSI LB+ | ETSI LB DRM | PR-ASK | 20 | 2.0 | 320 | Miller M=4 |
| **146** | **244** | **343** | ETSI LB+ | FCC DRM | PR-ASK | 20 | 2.0 | 250 | Miller M=4 |
| N/A | **205** | N/A | ETSI LB+ | Japan Ultra-DRM | PR-ASK | 20 | 2.0 | 50 | FM0 |
| **185** | **285** | **382** | ETSI LB+ | Sensitivity | PR-ASK | 20 | 2.0 | 160 | Miller M=8 |

*Supported Regions column indicates which regions a mode should pass regulatory certification tests on the Impinj E710 Development Board. The listed region is the most difficult region to pass, indicating that less difficult regions will also pass. For example, Mode 302 will pass ETSI upper band and FCC, but not Japan or ETSI lower band.

**Table 11: RAIN Gen2X Inventory Round Reader Mode IDs and Parameters**

| FCC Mode ID | ETSI LB Mode ID | ETSI UB Mode ID | Supported Regions* | Reader Mode Optimization | Forward Link Modulation | Tari (µs) | PIE | BLF (kHz) | Backscatter Link Modulation |
|---|---|---|---|---|---|---|---|---|---|
| 4124 | N/A | 4323 | ETSI UB+ | ETSI UB Hybrid | PR-ASK | 7.5 | 2.0 | 640 | BPSK M=2 |
| 4148 | N/A | 4345 | ETSI UB+ | ETSI UB Hybrid | PR-ASK | 7.5 | 1.5 | 640 | BPSK M=4 |
| 4123 | 4222 | 4324 | ETSI LB+ | ETSI LB Hybrid | PR-ASK | 20 | 2.0 | 320 | BPSK M=2 |

| FCC Mode ID | ETSI LB Mode ID | ETSI UB Mode ID | Supported Regions* | Reader Mode Optimization | Forward Link Modulation | Tari (µs) | PIE | BLF (kHz) | Backscatter Link Modulation |
|---|---|---|---|---|---|---|---|---|---|
| 4141 | 4241 | 4342 | ETSI LB+ | ETSI LB DRM | PR-ASK | 20 | 2.0 | 320 | BPSK M=4 |
| 4146 | 4244 | 4343 | ETSI LB+ | FCC DRM | PR-ASK | 20 | 2.0 | 250 | BPSK M=4 |
| 4185 | 4285 | 4382 | ETSI LB+ | Sensitivity | PR-ASK | 20 | 2.0 | 160 | BPSK M=8 |

*Supported Regions column indicates which regions a mode should pass regulatory certification tests on the Impinj E710 Development Board. The listed region is the most difficult region to pass, indicating that less difficult regions will also pass. For example, Mode 4345 will pass ETSI upper band and FCC, but not Japan or ETSI lower band.

#### 2.4.4.1 Inventory Read Rate Performance

Tag read rates for a large tag population in a quiet RF environment using Gen2 and Impinj Gen2X reader modes are shown in Table 12. Read rates for Impinj E910 reader chip are typically slightly higher, and Impinj E510 and E310 reader chips are typically lower. For more details, see the Impinj E710 Development Board Application Note. For information on selecting a Reader Mode, see the following support article: Selecting a Reader Mode for the Impinj Reader Chips.

Read rates for Gen2X reader modes with standard RN16 parameters are typically slightly lower than Gen2 reader modes with equivalent reader mode parameters. However, Gen2X link enhancements include configurable RN16 parameters, both numerical and error-reducing, that accelerate inventory by reducing ACK data and erroneous ACKs. They also include session-dependent RN16 protection that allows readers to discriminate which reader a tag's response is intended for, reducing cross-reads in multi-reader environments. For more details on Gen2X tag-to-reader link enhancements, please request support through the Impinj Support Portal at support.impinj.com.

**Table 12: Impinj E Family Reader Mode Read Rate Performance**

| Reader Mode ID* | Reader Mode Optimization | Forward Link Modulation | Tari (µs) | PIE | BLF (kHz) | Back-scatter Link Modulation | Typical Optimized Read Rate (tags/s) |
|---|---|---|---|---|---|---|---|
| **103** | FCC Read Rate | DSB-ASK | 6.25 | 1.5 | 640 | FM0 | 1100 |
| **302** | ETSI UB Read Rate | PR-ASK | 7.5 | 2.0 | 640 | FM0 | 950 |
| **120** | FCC Hybrid | DSB-ASK | 6.25 | 1.5 | 640 | Miller M=2 | 800 |
| **104** | FCC Read Rate | DSB-ASK | 6.25 | 1.5 | 320 | FM0 | 725 |
| **323** | ETSI UB Hybrid | PR-ASK | 7.5 | 2.0 | 640 | Miller M=2 | 700 |
| **203** | Japan Read Rate | PR-ASK | 12.5 | 1.5 | 426 | FM0 | 600 |
| **202** | ETSI LB Read Rate | PR-ASK | 15 | 2.0 | 426 | FM0 | 500 |
| **226** | Japan Hybrid | PR-ASK | 12.5 | 1.5 | 426 | Miller M=2 | 500 |
| **344** | ETSI UB DRM | PR-ASK | 7.5 | 2.0 | 640 | Miller M=4 | 450 |
| **345** | ETSI UB Hybrid | PR-ASK | 7.5 | 1.5 | 640 | Miller M=4 | 450 |
| **225** | ETSI LB Hybrid | PR-ASK | 15 | 2.0 | 426 | Miller M=2 | 425 |
| **224** | Japan Hybrid | PR-ASK | 12.5 | 1.5 | 320 | Miller M=2 | 400 |
| **223** | ETSI LB Hybrid | PR-ASK | 15 | 2.0 | 320 | Miller M=2 | 350 |
| **222** | ETSI LB Hybrid | PR-ASK | 20 | 2.0 | 320 | Miller M=2 | 300 |
| **241** | ETSI LB DRM | PR-ASK | 20 | 2.0 | 320 | Miller M=4 | 200 |
| **146** | FCC DRM | PR-ASK | 20 | 2.0 | 250 | Miller M=4 | 175 |
| **205** | Japan Ultra DRM | PR-ASK | 20 | 2.0 | 50 | FM0 | 95 |
| **285** | Sensitivity | PR-ASK | 20 | 2.0 | 160 | Miller M=8 | 70 |

| Reader Mode ID* | Reader Mode Optimization | Forward Link Modulation | Tari (µs) | PIE | BLF (kHz) | Back-scatter Link Modulation | Typical Optimized Read Rate (tags/s) |
|---|---|---|---|---|---|---|---|
| **4323** | ETSI UB Hybrid | PR-ASK | 7.5 | 2.0 | 640 | BPSK M=2 | 700 |
| **4345** | ETSI UB Hybrid | PR-ASK | 7.5 | 1.5 | 640 | BPSK M=4 | 450 |
| **4222** | ETSI LB Hybrid | PR-ASK | 20 | 2.0 | 320 | BPSK M=2 | 300 |
| **4241** | ETSI LB DRM | PR-ASK | 20 | 2.0 | 320 | BPSK M=4 | 200 |
| **4146** | FCC DRM | PR-ASK | 20 | 2.0 | 250 | BPSK M=4 | 150 |
| **4285** | Sensitivity | PR-ASK | 20 | 2.0 | 160 | BPSK M=8 | 65 |

*Reader mode availability shown for Impinj Reader Chip SDK+FW version 2.1. For a full listing of reader modes and parameters, see Table 10.

#### 2.4.4.2 Receive Sensitivity Performance

Table 14 through Table 17 show typical receive sensitivity for all four of the Impinj E Family reader chips in the reader circuit on the Impinj E710 Development Board.

These sensitivities are described at the chip Rx pin assuming 11 dB of path loss to the antenna, accounting for a 10 dB directional coupler and ~1 dB of miscellaneous path loss. To translate this data to the reader antenna port, add 11 dB.

This data is representative of the typical receive sensitivity as measured by a CISC Xplorer RAIN RFID sensitivity tester, using a 90% success rate and assuming a transmit power of 30 dBm.

The sensitivity in each reader mode is described in the hopping regional configuration the mode was primarily designed to operate in, as described in the “Mode Optimization” column. Reader mode 285 is described in the ETSI lower band region.

For the Impinj E910 and E710 chips, sensitivity in each reader mode is described assuming the baseband filter most appropriate for that mode, e.g. DRM filter for DRM modes, and high pass filter for other modes. The Impinj E510 and E310 are described assuming the high pass filter was used for all modes, as these parts are typically used in more integrated designs.

The sensitivity in each reader mode is described under four antenna conditions: Ideal, Typical, Handheld, and Poor antenna conditions. Each condition includes a cable delay and a return loss. Increased cable length de-correlates the local self-jammer reference from the actual self-jammer signal, making sensitivity worse. Increased return loss reduces the magnitude of the self-jammer and improves sensitivity. The return loss specified describes the apparent return loss of the fixed attenuation at the end of the delay cable, and does not include any loss from the delay cable. The non-ideal antenna conditions use a short-terminated return loss. The antenna conditions are described in Table 13.

Receive sensitivities for Impinj Gen2X reader modes are not shown here, as Gen2X receive sensitivity currently cannot be measured using the CISC Xplorer. The improved Gen2X BPSK backscatter modulation improves reader chip sensitivity by >3 dB. Optional symbol encoding further improves receive sensitivity by up to 2 dB. When operating in Gen2X inventory rounds, E Family-based readers will have improved reader sensitivity by 3 to 5 dB when compared to Gen2 reader modes with similar parameters. These sensitivity improvements are based on PER testing with the Impinj E710 Development Board and Impinj E Family reader chip SDK+FW version 2.1. For more details on the performance of Impinj Gen2X inventory rounds, see the Impinj Reader Chip Gen2X Inventory Application Note.

Table 13: Sensitivity Test Antenna Conditions

| Antenna Condition | Return Loss (dB) | Cable Length (meters) | Equivalent Delay at 865.7 MHz (ns) | Equivalent Delay at 927.25 MHz (ns) |
|---|---|---|---|---|
| **Ideal** | >22 | 1.07 | 5.99 | 6.01 |
| **Typical** | 15 | 1.52 | 8.12 | 8.15 |
| **Handheld** | 10 | 1.07 | 5.99 | 6.01 |
| **Poor** | 10 | 9.07 | 39.8 | 39.3 |

Table 14: Impinj E910 RAIN Gen2 Receive Sensitivity At Chip Rx Pin

| Reader Mode ID | Reader Mode Optimization | Forward Link Modulation | Tari (µs) | PIE | BLF (kHz) | Back-scatter Link Modulation | Typical Chip Rx Pin Receive Sensitivity (dBm) | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Ideal Antenna | Typical Antenna | Handheld Antenna | Poor Antenna |
| **103** | FCC Read Rate | DSB-ASK | 6.25 | 1.5 | 640 | FM0 | -87.5 | -82.0 | -81.5 | -67.5 |
| **302** | ETSI UB Read Rate | PR-ASK | 7.5 | 2.0 | 640 | FM0 | -88.5 | -85.5 | -81.5 | -71.5 |
| **104** | FCC Read Rate | PR-ASK | 15.0 | 2.0 | 320 | FM0 | -88.0 | -87.0 | -86.0 | -68.0 |
| **120** | FCC Hybrid | DSB-ASK | 6.25 | 1.5 | 640 | Miller M=2 | -90.0 | -84.5 | -83.0 | -70.0 |
| **203** | Japan Read Rate | PR-ASK | 12.5 | 1.5 | 426 | FM0 | -88.5 | -86.5 | -85.5 | -69.0 |
| **323** | ETSI UB Hybrid | PR-ASK | 7.5 | 2.0 | 640 | Miller M=2 | -91.0 | -88.0 | -85.5 | -75.0 |
| **226** | Japan Hybrid | PR-ASK | 12.5 | 1.5 | 426 | Miller M=2 | -91.0 | -89.5 | -88.5 | -72.5 |
| **224** | Japan Read Rate | PR-ASK | 12.5 | 1.5 | 320 | Miller M=2 | -93.0 | -89.0 | -88.0 | -74.0 |
| **202** | ETSI LB Read Rate | PR-ASK | 15 | 2.0 | 426 | FM0 | -90.0 | -85.5 | -81.0 | -70.5 |
| **225** | ETSI LB Hybrid | PR-ASK | 15 | 2.0 | 426 | Miller M=2 | -92.5 | -90.0 | -86.5 | -73.5 |
| **345** | ETSI UB Hybrid | PR-ASK | 7.5 | 1.5 | 640 | Miller M=4 | -94.5 | -89.5 | -90.5 | -78.0 |
| **344** | ETSI UB DRM | PR-ASK | 7.5 | 2.0 | 640 | Miller M=4 | -94.5 | -89.5 | -90.5 | -78.0 |
| **223** | ETSI LB Hybrid | PR-ASK | 15 | 2.0 | 320 | Miller M=2 | -93.0 | -86.5 | -84.5 | -72.0 |
| **222** | ETSI LB Hybrid | PR-ASK | 20 | 2.0 | 320 | Miller M=2 | -93.0 | -87.0 | -85.0 | -75.0 |
| **241** | ETSI LB DRM | PR-ASK | 20 | 2.0 | 320 | Miller M=4 | -96.5 | -90.5 | -89.0 | -77.0 |
| **146** | FCC DRM | PR-ASK | 20 | 2.0 | 250 | Miller M=4 | -95.5 | -91.0 | -89.5 | -78.0 |
| **205** | Japan Ultra DRM | PR-ASK | 20 | 2.0 | 50 | FM0 | -67.5 | -66.5 | -65.5 | -52.5 |
| **285** | Sensitivity | PR-ASK | 20 | 2.0 | 160 | Miller M=8 | -103.0 | -97.0 | -91.0 | -82.0 |

Table 15: Impinj E710 RAIN Gen2 Receive Sensitivity At Chip Rx Pin

| Reader Mode ID | Reader Mode Optimization | Forward Link Modulation | Tari (µs) | PIE | BLF (kHz) | Back-scatter Link Modulation | Typical Chip Rx Pin Receive Sensitivity (dBm) | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Ideal Antenna | Typical Antenna | Handheld Antenna | Poor Antenna |
| **103** | FCC Read Rate | DSB-ASK | 6.25 | 1.5 | 640 | FM0 | -82.0 | -80.0 | -80.0 | -67.5 |
| **302** | ETSI UB Read Rate | PR-ASK | 7.5 | 2.0 | 640 | FM0 | -83.0 | -81.5 | -80.5 | -71.5 |

| Reader Mode ID | Reader Mode Optimization | Forward Link Modulation | Tari (µs) | PIE | BLF (kHz) | Back-scatter Link Modulation | Typical Chip Rx Pin Receive Sensitivity (dBm) | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Ideal Antenna | Typical Antenna | Handheld Antenna | Poor Antenna |
| **104** | FCC Read Rate | PR-ASK | 15.0 | 2.0 | 320 | FM0 | -83.0 | -81.5 | -80.5 | -68.0 |
| **120** | FCC Hybrid | DSB-ASK | 6.25 | 1.5 | 640 | Miller M=2 | -85.0 | -83.5 | -81.0 | -70.0 |
| **203** | Japan Read Rate | PR-ASK | 12.5 | 1.5 | 426 | FM0 | -84.0 | -83.0 | -82.0 | -69.0 |
| **323** | ETSI UB Hybrid | PR-ASK | 7.5 | 2.0 | 640 | Miller M=2 | -85.5 | -84.5 | -82.5 | -75.0 |
| **226** | Japan Hybrid | PR-ASK | 12.5 | 1.5 | 426 | Miller M=2 | -86.5 | -85.5 | -84.5 | -74.0 |
| **224** | Japan Read Rate | PR-ASK | 12.5 | 1.5 | 320 | Miller M=2 | -86.5 | -85.5 | -84.5 | -73.5 |
| **202** | ETSI LB Read Rate | PR-ASK | 15 | 2.0 | 426 | FM0 | -85.5 | -84.0 | -81.0 | -70.5 |
| **225** | ETSI LB Hybrid | PR-ASK | 15 | 2.0 | 426 | Miller M=2 | -88.0 | -86.5 | -85.5 | -73.5 |
| **345** | ETSI UB Hybrid | PR-ASK | 7.5 | 1.5 | 640 | Miller M=4 | -90.0 | -89.5 | -87.0 | -78.0 |
| **344** | ETSI UB DRM | PR-ASK | 7.5 | 2.0 | 640 | Miller M=4 | -89.5 | -89.5 | -87.0 | -77.5 |
| **223** | ETSI LB Hybrid | PR-ASK | 15 | 2.0 | 320 | Miller M=2 | -88.0 | -85.5 | -84.0 | -72.0 |
| **222** | ETSI LB Hybrid | PR-ASK | 20 | 2.0 | 320 | Miller M=2 | -88.0 | -85.0 | -84.0 | -74.0 |
| **241** | ETSI LB DRM | PR-ASK | 20 | 2.0 | 320 | Miller M=4 | -90.5 | -88.5 | -88.5 | -76.5 |
| **146** | FCC DRM | PR-ASK | 20 | 2.0 | 250 | Miller M=4 | -91.0 | -90.0 | -89.0 | -78.0 |
| **205** | Japan Ultra DRM | PR-ASK | 20 | 2.0 | 50 | FM0 | -77.5 | -77.5 | -76.5 | -63.5 |
| **285** | Sensitivity | PR-ASK | 20 | 2.0 | 160 | Miller M=8 | -98.0 | -95.0 | -90.5 | -82.0 |

**Table 16: Impinj E510 RAIN Gen2 Receive Sensitivity At Chip Rx Pin**

| Reader Mode ID | Reader Mode Optimization | Forward Link Modulation | Tari (µs) | PIE | BLF (kHz) | Back-scatter Link Modulation | Typical Chip Rx Pin Receive Sensitivity (dBm) | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Ideal Antenna | Typical Antenna | Handheld Antenna | Poor Antenna |
| **120** | FCC Hybrid | DSB-ASK | 6.25 | 1.5 | 640 | Miller M=2 | -79.5 | -79.5 | -79.5 | -70.0 |
| **323** | ETSI UB Hybrid | PR-ASK | 7.5 | 2.0 | 640 | Miller M=2 | -80.5 | -79.0 | -78.5 | -73.5 |
| **226** | Japan Hybrid | PR-ASK | 12.5 | 1.5 | 426 | Miller M=2 | -81.5 | -80.5 | -80.0 | -72.5 |
| **224** | Japan Read Rate | PR-ASK | 12.5 | 1.5 | 320 | Miller M=2 | -81.5 | -80.0 | -79.0 | -73.0 |
| **225** | ETSI LB Hybrid | PR-ASK | 15 | 2.0 | 426 | Miller M=2 | -81.5 | -81.0 | -78.5 | -71.0 |
| **345** | ETSI UB Hybrid | PR-ASK | 7.5 | 1.5 | 640 | Miller M=4 | -84.5 | -84.0 | -83.5 | -77.5 |
| **344** | ETSI UB DRM | PR-ASK | 7.5 | 2.0 | 640 | Miller M=4 | -84.0 | -84.0 | -83.5 | -77.5 |
| **223** | ETSI LB Hybrid | PR-ASK | 15 | 2.0 | 320 | Miller M=2 | -82.0 | -81.5 | -80.5 | -72.0 |
| **222** | ETSI LB Hybrid | PR-ASK | 20 | 2.0 | 320 | Miller M=2 | -82.5 | -81.5 | -80.0 | -73.0 |
| **241** | ETSI LB DRM | PR-ASK | 20 | 2.0 | 320 | Miller M=4 | -86.0 | -85.5 | -84.0 | -76.5 |
| **146** | FCC DRM | PR-ASK | 20 | 2.0 | 250 | Miller M=4 | -86.0 | -86.0 | -85.5 | -77.5 |
| **205** | Japan Ultra DRM | PR-ASK | 20 | 2.0 | 50 | FM0 | -73.0 | -73.0 | -72.0 | -63.5 |
| **285** | Sensitivity | PR-ASK | 20 | 2.0 | 160 | Miller M=8 | -93.0 | -90.5 | -90.5 | -82.0 |

**Table 17: Impinj E310 RAIN Gen2 Receive Sensitivity At Chip Rx Pin**

| Reader Mode ID | Reader Mode Optimization | Forward Link Modulation | Tari (µs) | PIE | BLF (kHz) | Back-scatter Link Modulation | Typical Chip Rx Pin Receive Sensitivity (dBm) | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Ideal Antenna | Typical Antenna | Handheld Antenna | Poor Antenna |
| **224** | Japan Read Rate | PR-ASK | 12.5 | 1.5 | 320 | Miller M=2 | -74.0 | -74.0 | -73.0 | -70.5 |
| **223** | ETSI LB Hybrid | PR-ASK | 15 | 2.0 | 320 | Miller M=2 | -72.0 | -72.0 | -72.0 | -70.5 |
| **222** | ETSI LB Hybrid | PR-ASK | 20 | 2.0 | 320 | Miller M=2 | -74.5 | -74.0 | -74.5 | -71.0 |
| **241** | ETSI LB DRM | PR-ASK | 20 | 2.0 | 320 | Miller M=4 | -77.5 | -77.5 | -77.5 | -74.5 |
| **146** | FCC DRM | PR-ASK | 20 | 2.0 | 250 | Miller M=4 | -79.5 | -79.0 | -79.5 | -76.0 |
| **205** | Japan Ultra DRM | PR-ASK | 20 | 2.0 | 50 | FM0 | -64.5 | -65.0 | -64.0 | -63.5 |
| **285** | Sensitivity | PR-ASK | 20 | 2.0 | 160 | Miller M=8 | -84.5 | -85.0 | -84.5 | -80.5 |

#### 2.4.4.3 Impinj Gen2X Power Delivery

Powerup waveform shaping and extended Tari values allow E Family readers to deliver more power to tags, improving tag sensitivity up to 2 dB in both Gen2 and Gen2X inventory rounds.

Power Boost is an improved reader powerup waveform that delivers up to 2 dB additional power to supporting tag chips during powerup initialization, when they most need it. This additional initialization power increases overall tag chip operating sensitivity by up to a commensurate 2 dB. Extended Tari values further increase available power during reader commands. Power Boost and extended Tari values are available in both Gen2 and Gen2X inventory rounds.

For more information on enabling Power Boost and extended Tari values with E Family reader chips, please request support through the Impinj Support Portal at support.impinj.com.

### 2.4.5 Radio Specifications

**Table 18: Chip Receiver Specifications**

| Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|
| **Input frequency** | 860 | | 930 | MHz | RX and LO Ports |
| **Input impedance** | | 50 | | ohm | RX and LO ports |
| **Return loss** | 10 | | | dB | S11<br>RX and LO Ports |
| **IIP2 – In Band** | | +51 | | dBm | Receiver RF Front End |
| **IIP2 – Out of Band** | | +56 | | dBm | Receiver RF Front End |
| **IIP3 – In Band** | | +13 | | dBm | Receiver RF Front End |
| **IIP3 – Out of Band** | | +9 | | dBm | Receiver RF Front End |
| **E910 RX port self-jammer power** | | | +8 | dBm | Must also be 10 dB or more below LO port input power |
| **E710, E510, E310 RX port self-jammer power** | | | +11 | dBm | Must also be 7 dB or more below LO port input power |
| **LO port input power** | | | +18 | dBm | **Note:** Some applications may see better performance with a lower LO port input power |
| **RX sensitivity** | | See Table 10 | | | |

| Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|
| **RSSI measurement accuracy** | | +/- 1 | | dB | After per-board RSSI calibration, across a specific RSSI range which varies per-SKU.<br>For more detail, see the Impinj E910, E710, E510, and E310 Based Reader Calibration Application Note |
| **Phase measurement accuracy** | | +/- 5 | | degrees | Phase measurements have 180 degrees of phase ambiguity in non-FM0 modes |

## Table 19: Chip Transmitter Specifications

| Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|
| **Maximum TX power output capability** | +11 | | | dBm | Chip is guaranteed to produce ≥ +11 dBm in its highest power configuration |
| **TX output power regulatory compliant range** | +5 | | +11 | dBm | Across this chip output power range, regulatory compliance is guaranteed with external amplification up to the maximum power allowed in the region*<br>*Based on Impinj internal readers and DVB. Regulatory compliance can vary based on loop filter design, other components, and the use of and quality of the PA. Follow Impinj design recommendations for optimal performance.<br>Achieving regulatory compliance with Tx power >31.5 dBm requires further considerations on layout and design best practices. Impinj strongly recommends having >31.5 dBm designs reviewed by Impinj Support via our Support portal.<br>Below this range, reader overall output power must be reduced by 1 dB per 1 dB of chip transmit power to meet regulatory compliance.<br>For more detail, see the TX Path Attenuation section in the Impinj E710 Development Board Application Note |
| **TX output power analog dynamic range** | 30 | | | dB | **Note:** Optimal spectral performance is achieved at maximum chip TX power. See section 3.1 for details. |
| **TX port analog power step size** | N/A | 1 | N/A | dB | **Note:** Digital power control offers finer resolution |
| **TX power digital control resolution** | | 12 | | Signed bits | Linear control, full scale achieves maximum TX output power<br>For more detail, see the Impinj E910, E710, E510, and E310 Based Reader Calibration Application Note |

## Table 20: Chip Power Detectors

| Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|
| **RX and LO power detector input** | -15 | N/A | +18 | dBm | |
| **RX and LO power detector accuracy** | | +/- 0.5 | | dB | After calibration*<br>Input power +4 to +17 dBm |
| | | +/- 1.0 | | dB | After calibration*<br>Input power -6 to +4 dBm |

***Note:** The Impinj E Family SDK only calibrates the LO power detector, not the Rx power detector.

**Table 21: Chip Transmit Synthesizer**

| Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|
| **Frequency range** | 860 | N/A | 930 | MHz | |
| **Frequency grid** | | 100<br><br>125<br>250 | | kHz<br><br>kHz<br>kHz | Europe (ETSI 302 208) EU1, EU2, Japan<br>China, Korea<br>USA (FCC) |
| **Reference input frequency** | | 24 | | MHz | TCXO Specification |
| **Reference frequency tolerance** | | | 10 | ppm | TCXO Specification |
| **Reference input level** | 0.5 | | 1.5 | Vp-p | AC Coupled clipped sine wave<br>Alternate waveforms require external filtering, see section 3.6.1 |
| **PLL settling time** | | 1.5 | | ms | 100 kHz grid, recommended PLL loop filter configuration |
| **TX phase noise** | | -120 | | dBc/Hz | Δf = 250 kHz |
| | | -136 | | dBc/Hz | Δf = 1 MHz |
| | | -139 | | dBc/Hz | Δf = 3.7 MHz |
| **TX In-band spurious emissions** | | -82 | | dBc | RBW = 3 kHz, average detector |
| **TX out-of-band spurious emissions** | | -80 | | dBm | Excluding spurs listed elsewhere in this table<br>Across frequency range 0.047 to 2 GHz (all regions)<br>RBW = 100 kHz<br>Average Detector |
| **TX carrier second harmonic** | | -30 | | dBc | |
| **TX carrier third harmonic** | | -25 | | dBc | |
| **TX clock harmonic spurs** | | -70<br>-73 | | dBm<br>dBm | At 864 MHz<br>At 960 MHz<br>Harmonics of 96 MHz digital clock<br>RBW = 100 kHz |
| **TX clock sideband spurs** | | -80 | | dBc | +/- digital clock frequency (96 MHz) from carrier frequency |

### 2.4.6 Auxiliary Analog Specifications

**Table 22: Chip Auxiliary ADC Specifications**

| Parameter | Typ | Unit | Conditions |
|---|---|---|---|
| **Input Minimum** | 0 | volts | |
| **Input Maximum** | 1 | volts | |
| **Resolution** | 10 | Bits | Full scale |
| **DNL** | 2 | LSB | |
| **INL** | 4 | LSB | |
| **Input Impedance** | 10 | kohms | Measured relative to ground |
| **Sample Rate** | 100 | ksps | Limited by host communication rate |

**Table 23: Chip Auxiliary DAC Specifications**

| Parameter | Typ | Unit | Conditions |
|---|---|---|---|
| **Resolution** | 10 | Bits | |
| **Current Mode Output Minimum** | 0 | µA | |
| **Current Mode Output Maximum** | 100 | µA | |
| **Current Mode DNL** | 2 | LSB | |
| **Current Mode INL** | 2 | LSB | |

### 2.4.7 Memory Functional Specifications

**Table 24: Chip Memory Specifications**

| Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|
| **Flash write cycle endurance** | 10,000 | N/A | N/A | Write cycles | All flash pages including application, calibration, and stored settings |

### 2.4.8 IO Functional Specifications

**Table 25: Chip Digital IO Specifications**

| Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|
| **Input high voltage** | 2 | | VDD_IO | V | Input high voltage levels |
| **Input low voltage** | -0.3 | | 0.8 | V | Input low voltage levels |
| **Output high voltage** | VDD_IO - 0.1 | | | V | Output high voltage |
| **Output low voltage** | | | 0.4 | V | Output low voltage |
| **Output sink and source current** | 4 | | | mA | |
| **IO pull up resistance** | 34 | 51 | 81 | kohms | |

### 2.4.9 Host SPI Interface Functional Specifications

Table 26 contains the requirements of the host SPI interface. For more details on SPI configuration, see section 4.2.

**Table 26: Chip Host SPI Interface Specifications**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| **SPI Host Clock SCLK Frequency – Application** | 1.00 | 3.80 | 4.00 | MHz |
| **SPI Host Clock SCLK Frequency – Bootloader** | 0.90 | 0.95 | 1.00 | MHz |
| **SPI Host Clock SCLK Rise/Fall Time** | 330 | | | ps |
| **SPI Host Clock SCLK Duty Cycle** | 40 | 50 | 60 | % |
| **SPI Host Chip Select CS Setup Time** | 30 | | | ns |
| **SPI Host Chip Select CS Hold Time** | 3 | | | ns |
| **SPI Host Data Output MOSI Setup Time** | 30 | | | ns |
| **SPI Host Data Output MOSI Hold Time** | 3 | | | ns |
| **SPI Host Data Input MISO Valid Time** | | | 13 | ns |

# 3 FUNCTIONAL DESCRIPTION

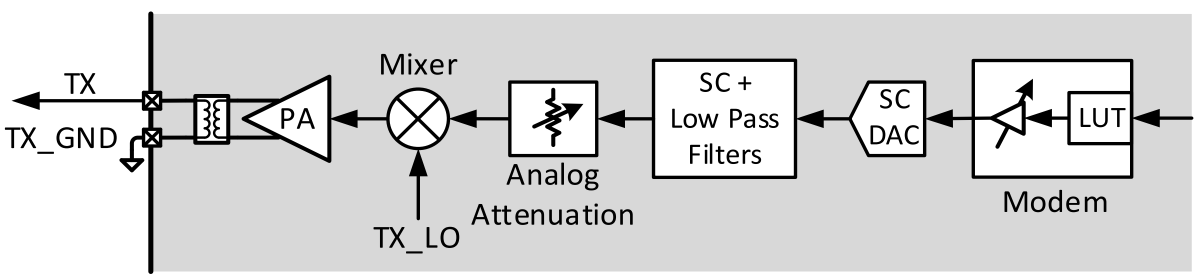
## 3.1 Analog Transmitter Path

The Impinj E910, E710, E510, and E310 reader chips contain the entire digital and analog TX signal chain required to transmit up to the maximum transmit power of the reader chips, as specified in Table 19. This signal chain is shown in Figure 10. An external power amplifier may be used in applications where additional transmit power is required.

The transmitted waveform is generated inside the modem, where a lookup table contains a sequence of digital values. Those digital values go through a digital multiplication with a signed 12-bit gain value (also known as “fine gain”). After the digital multiplication, the values enter a switched capacitor (SC) digital to analog converter (DAC), and exit as an analog waveform. The analog waveform goes through switched cap and low pass filters before an analog attenuation stage. The analog attenuation (also known as “gross gain”) has 30 ~1 dB attenuation steps. After attenuation, the analog waveform is mixed with the transmit local oscillator (TX_LO), and then amplified by the internal PA, and finally output through a balun as a single ended signal on the TX pin.

The Impinj E910, E710, E510, and E310 reader chips produce optimal spectral performance when the internal power amplifier is operated at the maximum allowable power (~11 dBm). The internal analog and digital gain can be reconfigured at runtime to cover a wide power range. Given the optimal spectral performance at high output power, the reader chip and surrounding circuitry, including external PA bias, should be configured to target maximum reader output power at the maximum chip output power. Then the overall output power can be reduced to lower values by reducing the internal chip analog gain. For more details on optimizing transmit power, including selecting external TX attenuation circuit values, see the Impinj E710 Development Board Application Note.

**Figure 10 – Transmitter Front End Analog Circuitry**



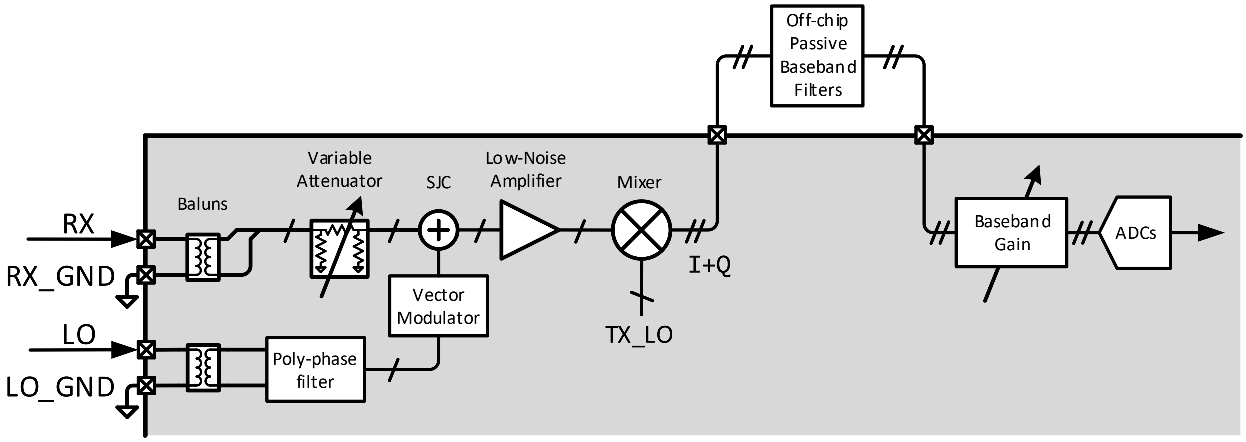

## 3.2 Analog Receiver Data Path

### 3.2.1 Receiver Front End Circuitry

The Receive (RX) and Local Oscillator (LO) RF inputs to the Impinj E910, E710, E510, and E310 reader chips are single ended, meaning no external balun is required to convert a single ended PCB trace signal to a differential signal for connection to the reader chip. Local RF ground signals are exposed at the adjacent pins (RX_GND and LO_GND), to optimize RF performance.

The Impinj E910, E710, E510, and E310 reader chip internal receiver circuitry is shown in Figure 11.

**Figure 11 – Receiver Front End Analog Circuitry**




### 3.2.2 Local Oscillator Input

The Local Oscillator (LO) input has a maximum input power, as described in Table 18. This means that in designs with high transmit powers, external attenuation may be required to reduce the incident power on the LO port. See the Impinj E710 Development Board Application Note for more details.

### 3.2.3 Self-Jammer Cancellation Block

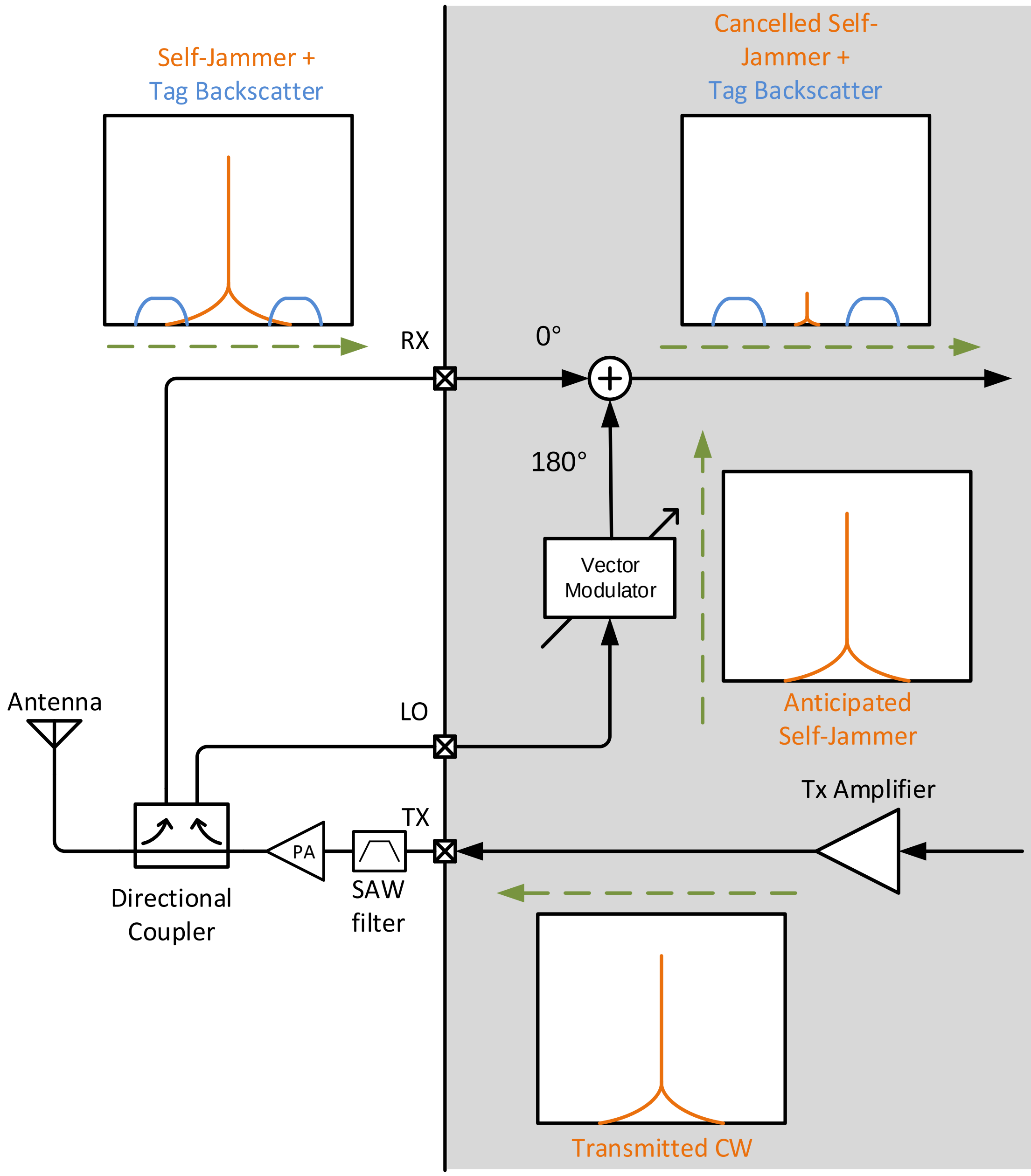
The Impinj E910, E710, E510, and E310 reader chips contain self-jammer cancellation (SJC) circuitry to improve receiver sensitivity. This circuit effectively reduces the negative impact of antenna reflection of the transmitted carrier wave (CW) on the receiver's sensitivity. RAIN systems using monostatic antenna configurations suffer from self-jammer problems because the transmitter must transmit CW continuously while the tags are backscattering their reverse link signal. That transmitted CW will reflect off of the antenna, resulting in a self-jammer signal incident at the receive port of the reader chip. That self-jammer signal will be much larger in amplitude than the reverse link signal from the tags.

The next-generation SJC block in the Impinj E910, E710, E510, and E310 reader chips iterate upon the SJC block developed in the Impinj Indy R2000 chip, reducing current consumption by implementing passive self-jammer cancellation, and improving sensitivity by increasing the resolution of the vector modulator circuit.

The Impinj E910, E710, E510, and E310 reader chips perform self-jammer cancellation by converting the Local Oscillator (LO) signal into an anticipated reflected CW and subtracting it from the Receive (RX) signal, using the Vector Modulator and other components shown in Figure 11. An example of the complete signal chain and resultant receive signal spectrum is shown in Figure 12.

Proper operation of the SJC requires that the LO signal have the proper amplitude as it enters the Impinj E910, E710, E510, and E310 reader chips, as shown in the electrical specs in Table 18. In most applications, this will require the use of additional passive attenuation outside of the reader chip. For examples of this circuit configuration, see the Impinj E710 Development Board Application Note.

**Figure 12 – Self Jammer Cancellation Spectrum**




### 3.2.4 Receive Baseband Interface

After the self-jammer signal is removed from the receive signal, the resulting RF signal is demodulated using the LO, resulting in a quadrature baseband signal. This signal is then filtered to remove out of band frequency content. The unfiltered signal is output from the reader chip on the differential quadrature MIX_... pins, and after external passive baseband filtration, it re-enters the reader chip through the differential quadrature AMP_... pins. The filtered baseband signal is then further amplified and filtered inside the reader chip, and finally digitized in on-chip ADCs to be processed by the modem. This arrangement is shown in Figure 13.

The component topology and values for the off-chip baseband filters vary by application. For recommendations, see the Impinj E710 Development Board Application Note. In some configurations, baseband signal filtering is not required, but in all cases the design should have at minimum DC blocking capacitors to interface between the receive mixer and the amplifiers before the ADC.

The reader chips have a single set of differential quadrature input and output pins, so if multiple passive filter networks are desired, external RF switching must be added to the circuit, as demonstrated on the Impinj E710 development board.

The individual mixer output and amplifier input pins each have configurable series resistors inside the part, with a resistance of either 250 or 1000 Ω on each input or output pin, as configured by the firmware using the field **`HpfMode`** in register **`HpfOverrideSettings`**. This is shown in Figure 14. Note that because there are two resistors, they produce either 500 or 2000 Ω total series resistance, matching the SDK description of the pin configuration in the **`HpfOverrideSettings`** register.

Impinj's implementation of the SDK uses the 250 Ω resistance to match the 500 Ω characteristic impedance baseband filters implemented on the Impinj E710 development board.

**Figure 13 – Receive Baseband Interface**

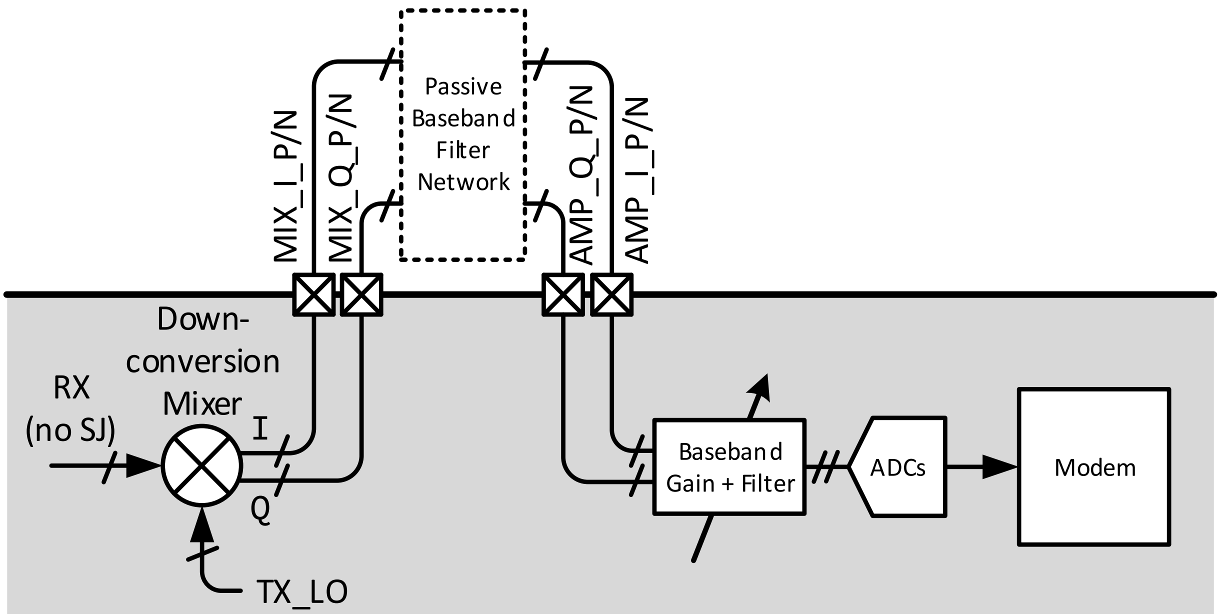
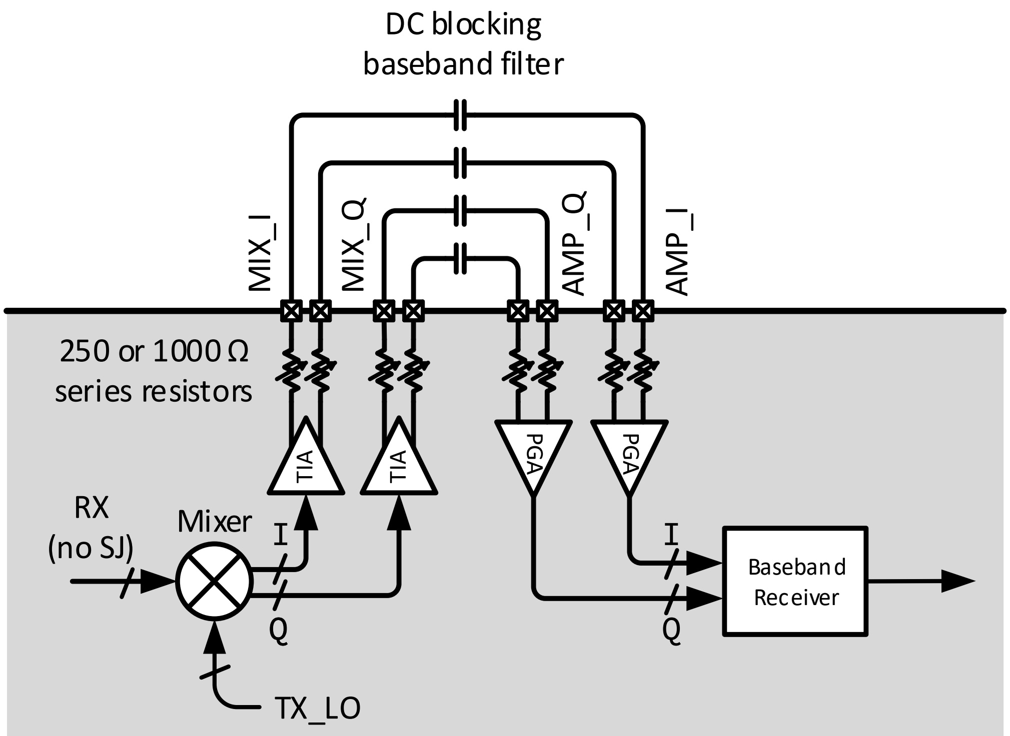


**Figure 14 – Receiver Baseband Filter Pin Interface Detail**




## 3.3 Antenna Configuration Scenarios

The Impinj E910, E710, E510, and E310 reader chips can be configured for monostatic (single antenna used for both transmit and receive) or bistatic (separate antennas used for transmit and receive) operation. Monostatic configurations are generally more popular, because of the lower cost and size of a single antenna system, but bistatic configurations have the advantage of increased receive sensitivity due to the smaller self-jammer signal on the receive antenna.

The Impinj E910, E710, E510, and E310 reader chips can also be configured for operation with multiple monostatic antennas, for example in a system with multiple physical zones, each with their own antennas. This can be accomplished using an external RF switch, also known as a multiplexer (mux), at the transmitted port of the directional coupler. The RF switch can be controlled by specific GPIOs. This arrangement is shown in Figure 17.

Figure 15 – Monostatic Antenna Configuration

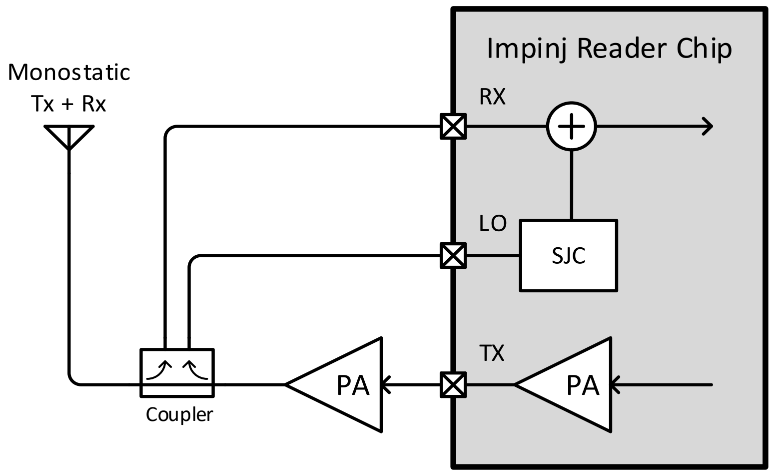



Figure 16 – Bistatic Antenna Configuration

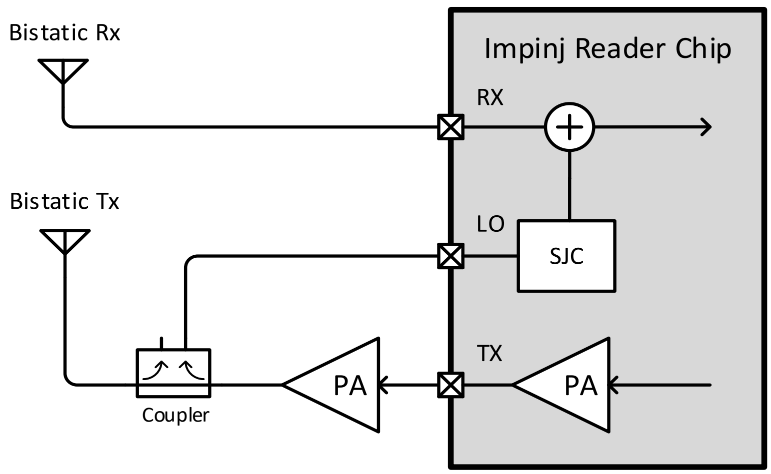
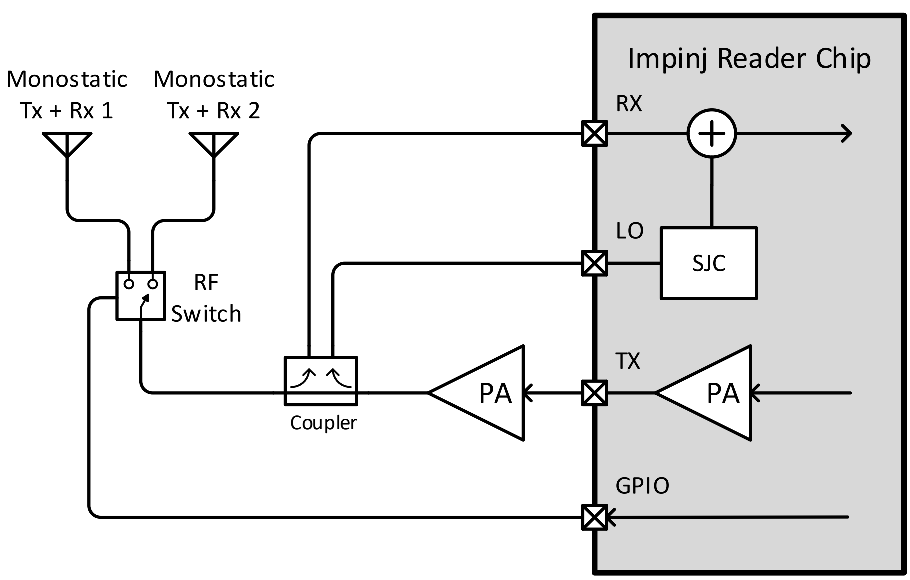


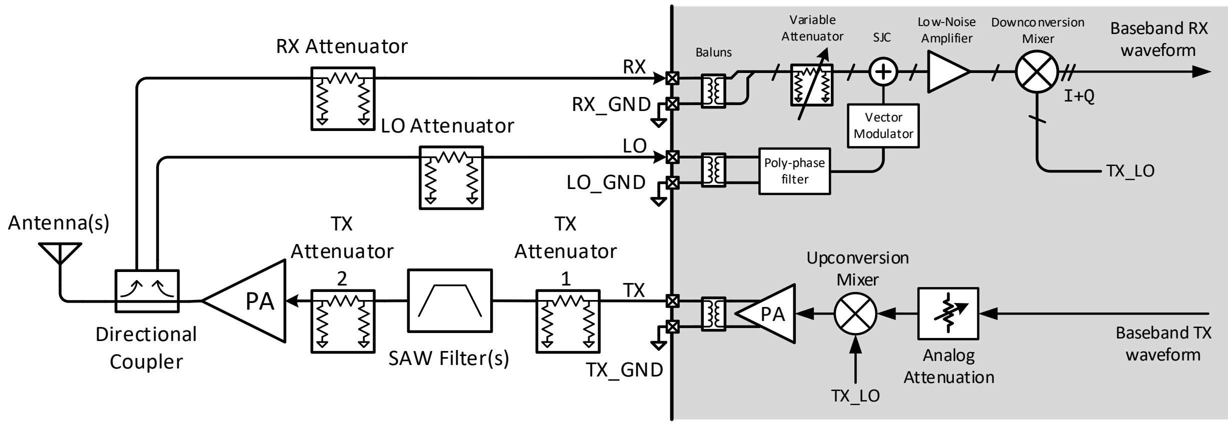

Figure 17 – Multiple Monostatic Antennas With RF Switch



## 3.4 RF TX, LO, and RX Path Configuration

The Impinj E910, E710, E510 and E310 reader chips' transmit (TX), local oscillator (LO), and receive (RX) pins must be connected to the antenna(s) via RF Front End circuitry to successfully implement a RAIN RFID reader. This circuitry potentially includes attenuators, one or more SAW filters, DC blocking series capacitors, one or more power amplifiers, one or more directional couplers, optional RF switches, and passive filters. All these components serve different purposes that are explained in detail in the [Impinj E710 Development Board Application Note](). A simplified example circuit is shown in Figure 18.

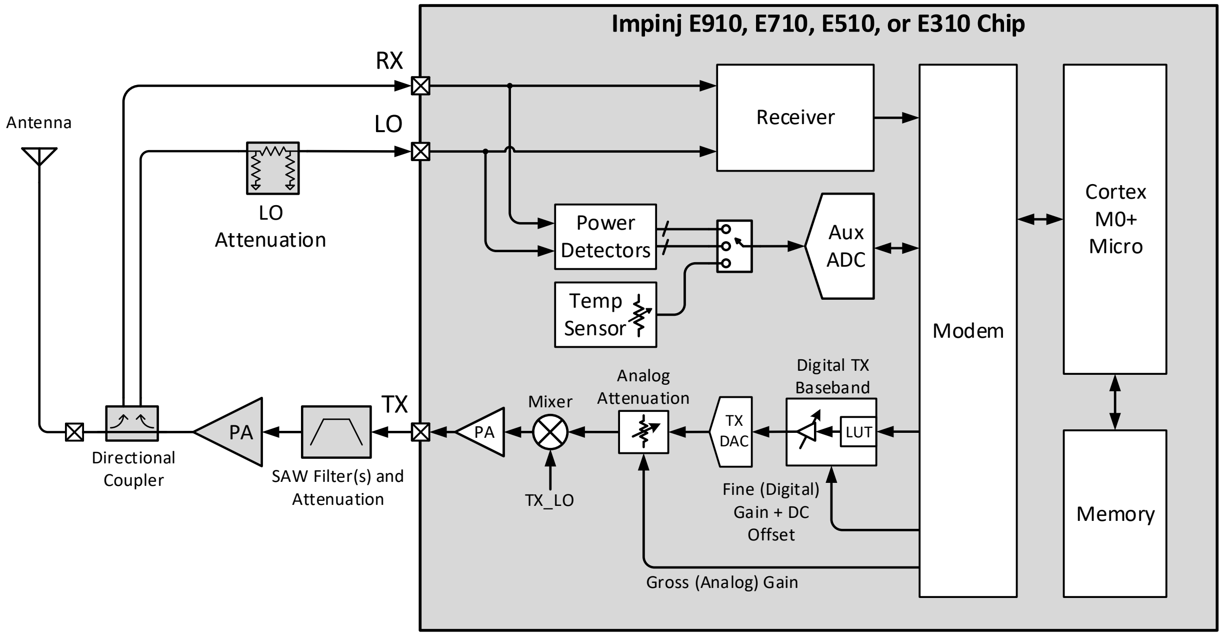
**Figure 18 – RF Front End Block Diagram**




## 3.5 RF Power Detection

The Impinj E910, E710, E510, and E310 reader chips contain power detectors connected to the RX and LO pins, allowing measurement of forward (transmit) power on the LO pin and reverse (self-jammer) power on the RX pin. These power detectors convert the RF power level at the RX and LO pins into analog voltages, which are measured by the Auxiliary ADC inside the reader chips. LO power measurements are used to measure the forward power for closed loop transmit power control via the fine gain in the transmitter. This arrangement is shown in Figure 19. These sensors require some calibration in circuit because circuit design and component values will alter the transfer function between the desired quantities and the power at the reader chip pins. For more detail on calibration and closed loop power control, see the Impinj E910, E710, E510, and E310 Based Reader Calibration Application Note.

Figure 19 – Impinj Reader Circuit Block Diagram With Sensors




## 3.6 Frequency Generation

### 3.6.1 Temperature Compensated Crystal Oscillator

The Impinj E910, E710, E510 and E310 reader chips require a high accuracy clock reference signal from an external temperature compensated crystal oscillator (TCXO) to be used as a reference for the voltage-controlled oscillator and phase-locked loop internal to the reader chip. The TCXO clock output signal is fed into the reader chip via the high impedance FREF pin. The FREF pin requires AC coupling to remove the DC bias voltage of the TCXO output. The Impinj E710 development board uses a 1 nF capacitor, but other TCXOs may require a different component value. Some TCXO components require a specific load to operate, and this may require external passive components to implement.

TCXO selections should meet the requirements listed in the electrical specifications, specifically Table 21, including the frequency, PPM error, and output waveform's shape and peak to peak voltage. If the peak-to-peak voltage exceeds the specifications of the reader chip, it can be reduced using a voltage divider circuit before the AC coupling capacitor. If necessary, Impinj recommends using a resistor voltage divider with a series resistance of 1 kΩ, and an appropriately scaled shunt resistance for the waveform amplitude. If the waveform shape is not a clipped sine wave, for example a CMOS or HCMOS square wave, it may need to be low-pass filtered using an RC circuit to reduce higher order frequency content, as these can couple into the transmitter and receiver and degrade performance. The TCXO power supply can likewise contain high frequency noise and may require some electrical isolation from the reader circuit.

An example TCXO circuit is shown in Figure 20.

Other TCXO specifications that may matter in the reader system include startup time, power consumption, frequency stability over time, voltage, temperature, and load, etc. These specifications must be considered in reader design, as they may have design implications.

Some TCXO devices are "pullable" meaning a voltage can be applied to one of their pins to shift the operating frequency. This may be used as a mechanism of frequency calibration. If this behavior is not desired, the pin should be driven to the appropriate DC value to disable frequency pulling.

Impinj has used the following TCXOs with success:

- TXC 7Q-24.000MBN-T
- Taitien TXEABLSANF-24.000000

- [Abracon ASTX-H11-24.000MHZ-T]
    - Note: Requires an output voltage divider to achieve <1.5 $V_{P-P}$ input level
    - Impinj achieved this using a resistor voltage divider including 1 kohm series resistor and a 432 ohm shunt resistor, followed by a 1 nF series capacitor at the FREF pin

### 3.6.2 Voltage Controlled Oscillator

The Impinj E910, E710, E510 and E310 reader chips contain a voltage-controlled oscillator (VCO) that generates a ~3.6 GHz reference signal. The reference signal is subsequently divided by 4 to generate the carrier wave (CW) signal used for RF transmission, also known as the Transmit LO (Local Oscillator) signal. This reference signal is tunable, allowing the reader chips to operate in different channels in multiple regulatory regions. The VCO is tuned using closed loop feedback from the phase-locked loop (PLL), using the TCXO output as a reference clock.

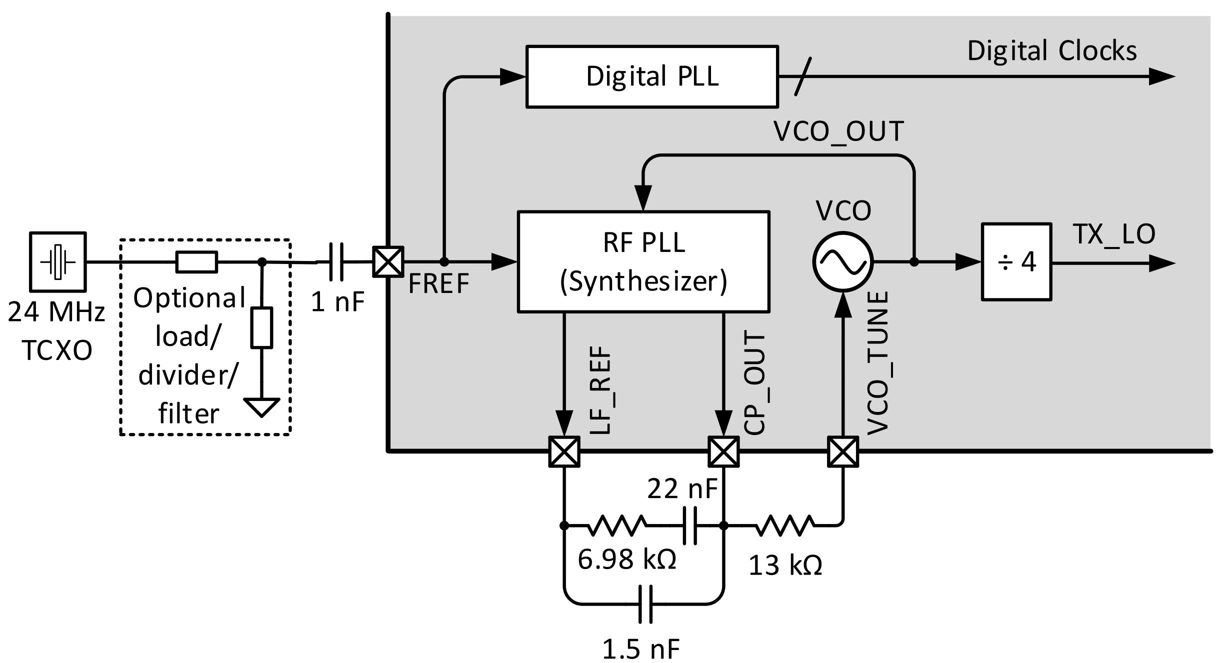
The VCO and phase-locked loop circuits are configured by the reader chips' embedded firmware image. The SPI host can interact with this configuration via Operations and Register values. This is demonstrated in the SDK's examples, as described in the Impinj Reader Chip SDK Documentation.

### 3.6.3 PLL Loop Filter

In addition to the VCO, the Impinj E910, E710, E510 and E310 reader chips have a built-in phase-locked loop (PLL) circuit, which allows automatic tuning of the VCO to a specific desired frequency, using the 24 MHz TCXO clock input as a reference. The PLL requires an external loop filter made up of passive components to provide optimum performance. The external TCXO output signal must also be connected to the FREF input as described above in section 3.6.1 - Temperature Compensated Crystal Oscillator. The recommended circuit components and topology are shown in Figure 20.

Impinj recommends that partners use the specific component values and tolerances that are used in the Impinj E710 development board. The BOM for the development board can be downloaded from our support portal here: https://support.impinj.com/hc/en-us/articles/360011416140

**Figure 20 – PLL Block Diagram and Loop Filter Topology**



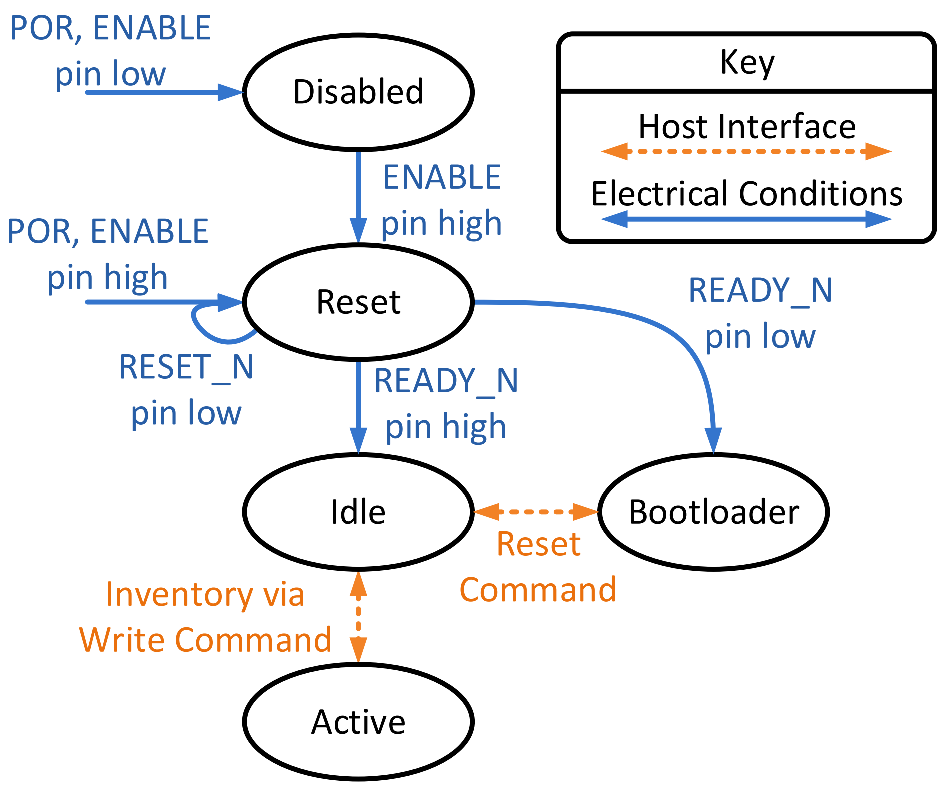
## 3.7 Power Modes

The Impinj E910, E710, E510, and E310 reader chips have multiple operating modes, allowing power consumption and performance optimizations for all applications. The power modes and transitions between them are shown in Figure 21. Power consumption characteristics of the modes are shown in Table 8.

When power is applied to all of the power supply pins on the reader chip, it will enter either Disabled or Reset power mode, depending on the state of the ENABLE pin. If the ENABLE pin is low, it will enter the Disabled mode, but if the ENABLE pin is high, it will enter the Reset mode. From the Reset mode, if the RESET_N pin is high, the reader chip will transition into either the Idle or Bootloader mode, depending on the state of the READY_N pin. The READY_N pin can be driven low to force the reader chip into the Bootloader mode or left high to allow the reader chip to boot into Idle mode. From Idle mode, the reader chip can be sent into the Active mode(where RFID operations are performed) or Bootloader mode, depending on commands sent via the host interface. The RESET_N pin can be used at any time to force the reader chip into the Reset mode or keep it there indefinitely. Setting the ENABLE pin low will force the reader chip into the Disabled power mode, which consumes less current than any of the other power modes. Refer to section 2.3 - Power Supply for details on power mode transitions.

The Impinj E910, E710, E510, and E310 reader chips do not have an independent internal clock source, and if no 24 MHz clock signal is provided at the FREF input, the parts will not start up.

**Figure 21 – Impinj Reader Chip Power Modes**




# 4 DEVICE CONTROL AND PROGRAMMING

The Impinj E910, E710, E510, and E310 reader chips have an embedded Cortex-M0 microcontroller that runs RAIN application specific firmware provided by Impinj. That firmware implements the behavior necessary to operate the RAIN radio and exposes an interface for communication with a host device. The host device communicates with the reader chip over an SPI channel, implementing a specific communication scheme that is explained further below. Impinj provides explicit documentation of the "wireline" details of the protocol, enabling users to implement their own code to communicate with the reader chip. Impinj also provides an example implementation of a host library designed to communicate with the reader chip.

The Impinj E910, E710, E510, and E310 reader chips' embedded microcontrollers can only run the Impinj provided firmware images and will not execute any other application code. The reader chip exposes a firmware update interface(bootloader), so that newer versions of the firmware can be installed on the reader chip, adding new features, fixing bugs, etc. In addition to the RAIN behavior, the firmware also implements test and calibration functionality, and allows the non-volatile storage of calibration configuration, as well as stored configurations for RAIN behavior.

The Impinj E910, E710, E510, and E310 reader chips are populated with a firmware image during Impinj's manufacturing and test process. Impinj will populate with the latest major revision of firmware. The major revision is updated when large changes are made to the host interface, new reader chip devices are added, or major bugs are fixed. These major revision updates will be communicated to partners via PCN. Readers containing the Impinj E910, E710, E510, and E310 reader chips should include the capability to update the firmware image on the reader chip in the field, so that bugs can be removed, and new features can be added. Firmware updates should also be implemented during reader manufacturing flow, guaranteeing a specific firmware image version. For more information on performing firmware updates, see the Impinj Reader Chip SDK Documentation.

Further detail on the behavior of the embedded microcontroller is contained within the Impinj Reader Chip SDK Documentation. This document contains information on the structure of the data that is sent across the SPI communication interface, as well as the commands and responses that can be exchanged. It also contains a map of the registers that are used to read and write device configuration. It will document the functional behavior of the reader chip, including all the different operating modes the device supports.

## 4.1 Reader Communication Protocol

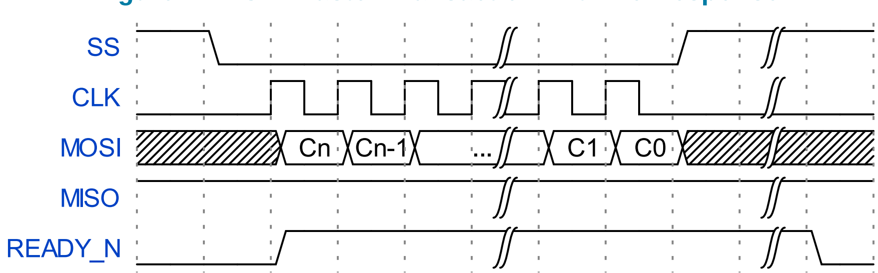
Impinj E910, E710, E510, and E310 reader chip communication with an SPI master host uses bytes that are sent across the SPI interface to build messages. These messages can describe commands from the host to the reader chip, and optionally responses from the reader chip to the host. Commands begin with a single "ID" byte, and responses begin with a single "response code" byte, and both are optionally followed by a payload made up of one or more fields of data, each broken up into a number of individual bytes. Not all commands have responses, but they will often change the state of the device registers. More detail on the reader communication protocol is contained in the Impinj Reader Chip SDK Documentation.

## 4.2 SPI Digital Communication Interface

The Impinj E910, E710, E510, and E310 reader chips communicate via SPI (Serial Peripheral Interface). The reader chip acts as an SPI slave. The reader chip has additional digital IOs that help coordinate SPI communication with the host, including the READY_N and IRQ_N pins.

The SPI uses 8-bit words, communicated most significant bit first. If multiple bytes are sent, they are sent with the most significant byte first. Both are "big endian". The SPI CPOL = 0, which means the clock signal SCLK idles low. The SPI CPHA = 1, which means the data pins MOSI and MISO states should change on the rising edge of the clock, and be sampled on the falling edge of the clock. For more details on the SPI timing parameters, see section 2.4.9. Some host devices may require a ~1k Ω pulldown resistor on the SCLK signal depending on their configuration.

Figure 22 – SPI Master Transaction With No Response



For more details on Impinj E910, E710, E510, and E310 reader chip SPI behavior and the host communication protocol, see the Impinj Reader Chip SDK Documentation.

### 4.3 Digital Input/Output Pins

The Impinj E910, E710, E510, and E310 reader chips have Digital Input/Output pins (DIGITAL_IOs) that can be used as digital inputs or outputs in certain configurations, for example for switching between antennas, SAW filters, or baseband receive filters, or reading external voltages. For more detail on controlling the Digital IOs, see the Impinj Reader Chip SDK Documentation.

## 5 PERFORMANCE CHARACTERISTICS

### 5.1 RX Sensitivity Summary

Receive sensitivity varies with many design parameters, including components used in the RF front end, the baseband filter, power supply topology, selected reader mode, etc. The RX sensitivity of the Impinj E710 development board has been captured in the Impinj E710 Development Board Application Note.

For more details on optimizing RX sensitivity, see the Impinj Reader Chip RF Performance Optimization Application Note.

### 5.2 Transmit Output Spectral Summary

Transmit output spectrum will vary by RF Mode (Link Profile) and external reader hardware. There is more detail on the transmit spectral performance in the Impinj E710 Development Board Application Note.

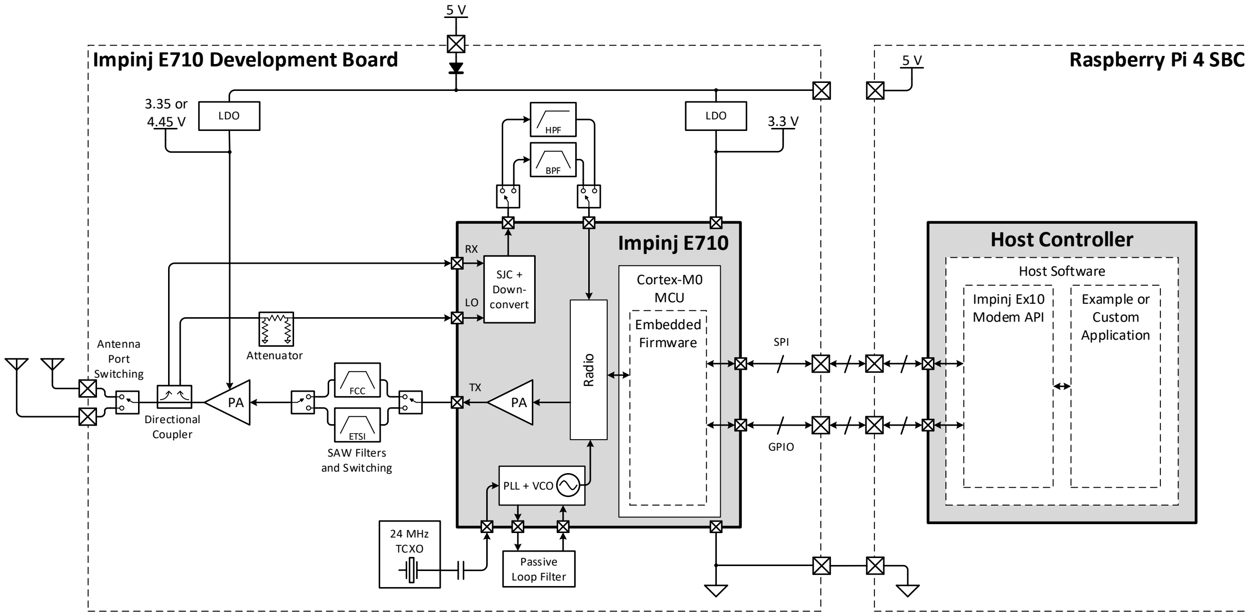
### 5.3 Transmit Power Control

The Impinj E910, E710, E510, and E310 reader chips have configurable transmit power gain, allowing run-time reconfiguration of the RAIN reader's transmit power. This system transmit power requires calibration to improve accuracy. For more detail on transmit power control and calibration, see the Impinj E910, E710, E510, and E310-Based Reader Calibration Application Note.

## 6 IMPINJ E710 DEVELOPMENT BOARD

For more application specific details on hardware configuration of the Impinj E910, E710, E510, and E310 reader chips, see the development board documentation, including the Impinj E710 Development Board Application Note. Figure 23 shows a detailed internal block diagram of the Impinj E710 development board and Raspberry Pi Host Single Board Computer (SBC).

## Figure 23 – Impinj E710 Development Board System Detailed Block Diagram

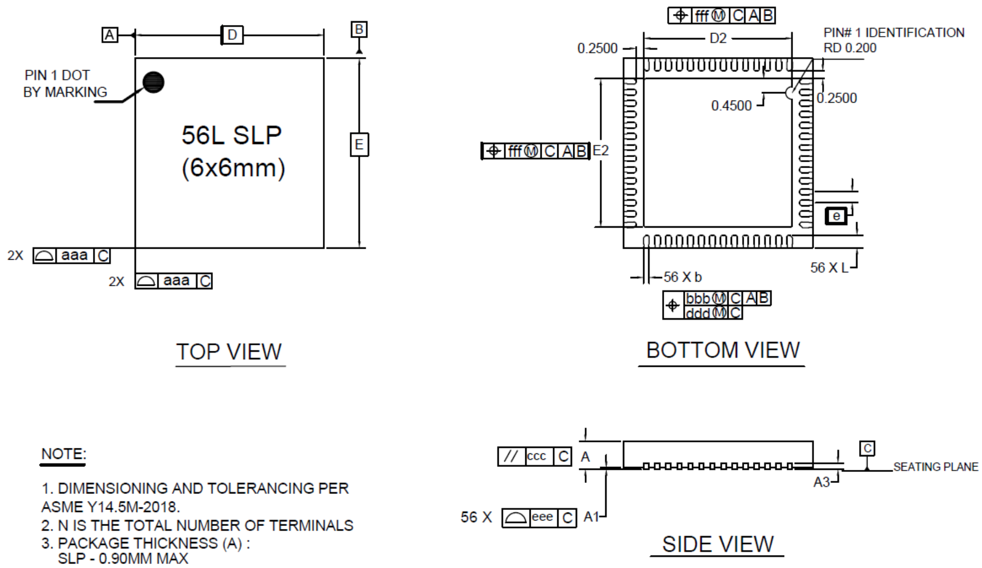


# 7 PACKAGE AND LAYOUT INFORMATION

## 7.1 Package Dimensions

The E Family reader chips are packaged in a 6 x 6 mm, 0.85 mm thick, 56-pin leadless sawn QFN package with a center e-pad that is connected to ground. The pins are spaced at a 0.35 mm pitch, center to center. The package and pin dimensions are shown in Figure 24.

**Figure 24 – Impinj Reader Chip Package and Pin Dimensions**



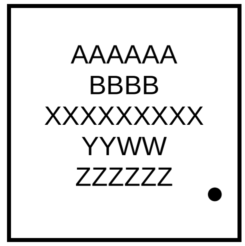

| Dimensional Ref. | | | |
|---|---|---|---|
| REF. | Min. | Nom | Max. |
| A | 0.800 | 0.850 | 0.900 |
| A1 | 0.000 | — | 0.050 |
| A3 | 0.203 REF | | |
| D | 6.000 BSC | | |
| E | 6.000 BSC | | |
| D2 | 4.600 | 4.700 | 4.800 |
| E2 | 4.600 | 4.700 | 4.800 |
| b | 0.130 | 0.180 | 0.230 |
| e | 0.350 BSC | | |
| L | 0.350 | 0.400 | 0.450 |
| Dimensional Tol. | | | |
| aaa | 0.100 | | |
| bbb | 0.070 | | |
| ccc | 0.100 | | |
| ddd | 0.050 | | |
| eee | 0.080 | | |
| fff | 0.100 | | |

**Note:** These dimensions describe the latest version of the package. Previous versions had slightly different package thickness and lead length specifications. For more details, see our Product Information Notification here: https://support.impinj.com/hc/en-us/articles/4418337492755

## 7.2 Package Markings

The markings on the Impinj E Family reader chip package are shown in Figure 25 and enumerated in Table 27. Note the pin 1 marking is in the lower right corner, relative to the text.

**Figure 25 – Impinj Reader Chip Package Markings**




**Note:** Drawing is not to scale

**Table 27: Impinj E Family Reader Chip Package Markings Encoding**

| Field | Definition |
|---|---|
| **AAAAAA** | "IMPINJ" or "PI" depending on lot |
| **BBBB** | Reader Chip Model Number (e.g. "E710") |
| **XXXXXXXXX** | Lot Number |
| **YYWW** | Date code (year and workweek) |
| **ZZZZZZ** | Country of origin |

## 7.3 PCB Layout Recommendations

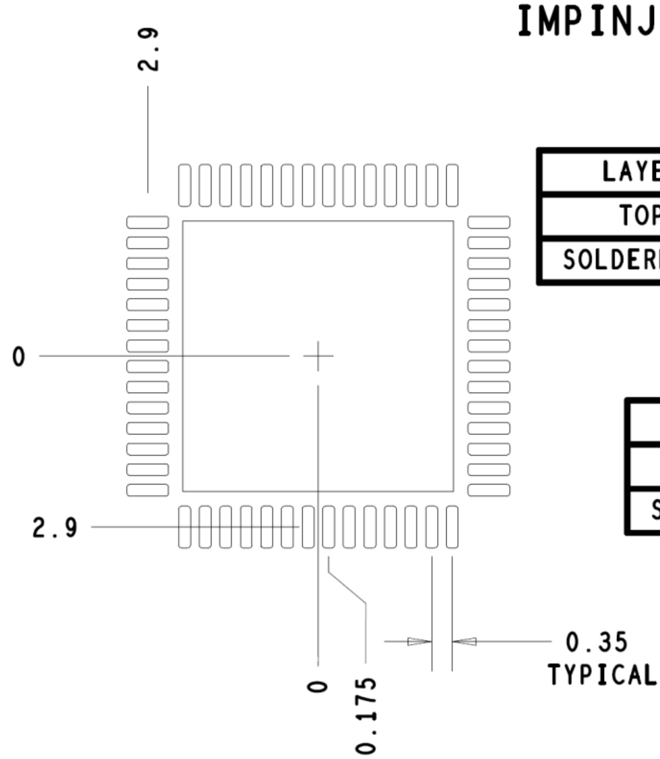
### 7.3.1 Recommended PCB Footprint

Impinj has implemented a recommended PCB footprint in our Impinj E710 Development Board, the Altium source for which can be downloaded from our support portal here: [https://support.impinj.com/hc/en-us/articles/360011416140](https://support.impinj.com/hc/en-us/articles/360011416140)

Impinj's recommended footprint pad dimensions are shown in Figure 26 and solder paste dimensions are shown in Figure 27.

**Figure 26 – Recommended PCB Footprint Pad and Soldermask Dimensions**

IMPINJ RECOMMENDED PAD PATTERN



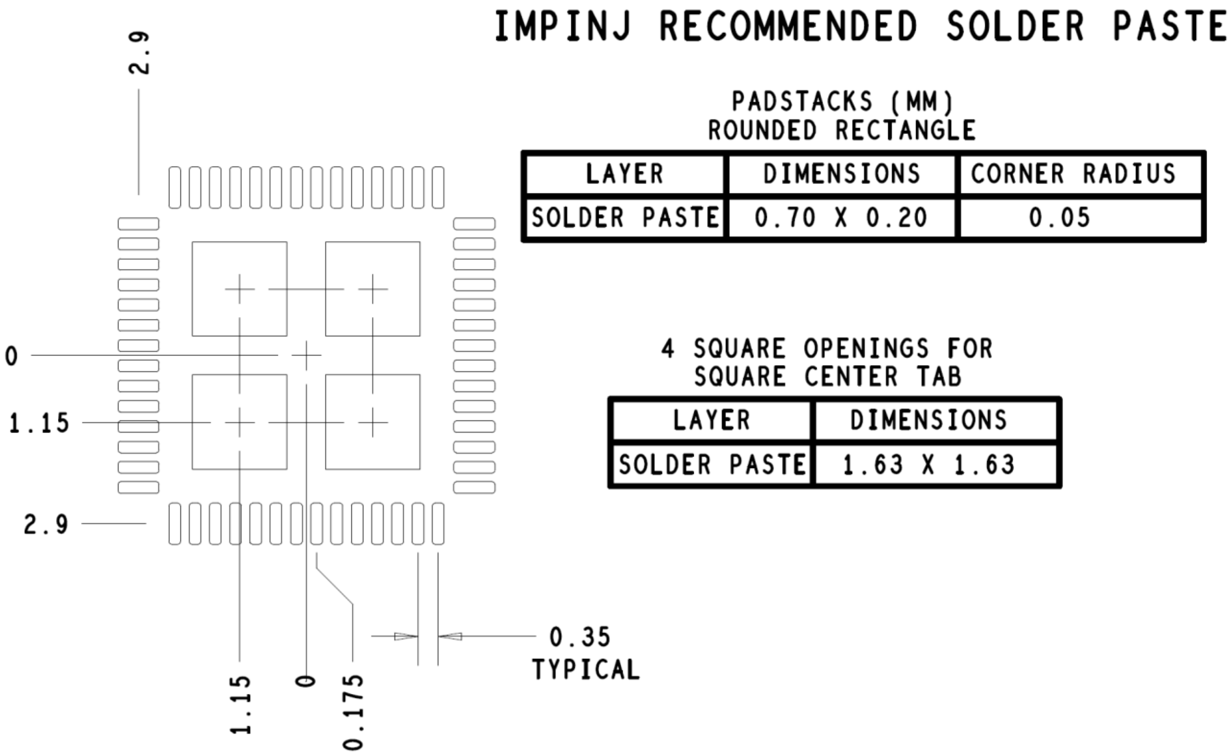

PADSTACKS (MM)
ROUNDED RECTANGLE

| LAYER | DIMENSIONS | CORNER RADIUS |
|---|---|---|
| TOP | 0.70 X 0.20 | 0.05 |
| SOLDERMASK | 0.81 X 0.365 | 0.075 |

SQUARE CENTER TAB

| LAYER | DIMENSIONS |
|---|---|
| TOP | 4.70 X 4.70 |
| SOLDERMASK | 4.80 X 4.80 |

Figure 27 – Recommended PCB Footprint Solder Paste Dimensions




## 7.3.2 Additional PCB Layout Recommendations

Radio circuit performance can vary widely depending on the routing of signals on the PCB. This section contains a series of recommendations to optimize PCB layout.

The RF signal paths of the radio circuit (including the TX, LO, and RX signals) should all be made up of 50-ohm characteristic impedance traces. This will minimize signal reflections and optimize reader efficiency and sensitivity. Although the baseband filter has a characteristic impedance, the signal frequencies are low enough that the traces do not need to be controlled impedance. The three signal paths should also be isolated from each other and from other signals on the PCB as much as possible, separated by ground fills on all possible layers.

PCB layout has a large impact on thermal circuit performance. The electrical conductivity of the traces, vias, and fills that make up the layers of a PCB also makes them very thermally conductive. Both the PA and Impinj E910, E710, E510, and E310 reader chips will self-heat as they consume electrical power. The reader chip and most PA components have large ground paddles or multiple ground pins to help conduct heat out of the ICs. These pins and paddles should be thermally and electrically connected to the ground fills of the reader board, using a healthy number of vias to cross from layer to layer where necessary. To further improve thermal performance in high-power applications, the ground fills of the reader PCB should be connected to a heat sink or chassis for dissipation into the surrounding environment.

All of the ground leads on the Impinj E910, E710, E510, and E310 reader chips, including the RF TX_GND, LO_GND, and RX_GND, should be tied directly to the PCB's ground net, via direct traces to the large thermal and electrical ground paddle corresponding to the e-pad in the center of the QFN package. This will ensure optimal RF, electrical, and thermal performance.

For an example of optimal layout for an Impinj E910, E710, E510, or E310 based RAIN RFID reader circuit, and more PCB layout guidance, see the Impinj E710 Development Board Application Note.

## 7.4 Recommended Reflow Profile

Impinj recommends a JEDEC standard J-STD-020 profile with a peak temperature of between 245° C and 250° C, with the characteristics listed in Table 28.

**Table 28: Recommended Reflow Profile Parameters**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| **Temperature Ramp Up Rate** | | | 3 | ° C / second |
| **Preheat Temperature** | 150 | | 200 | ° C |
| **Preheat Time** | 60 | | 180 | seconds |
| **Liquidus Temperature** | | 217 | | ° C |
| **Time above Liquidus Temperature** | 60 | | 150 | seconds |
| **Peak Temperature** | 245 | | 250 | ° C |
| **Time within 5° C of Peak Temperature** | 20 | | 40 | seconds |
| **Temperature Ramp Down Rate** | | | 6 | ° C / second |
| **Time Between Room Temp and Peak Temperature** | | | 480 | seconds |

# 8 TERMINOLOGY

Table 29 contains a list of relevant terminology and acronyms specific to RF systems and RAIN embedded readers.

**Table 29: Relevant Terminology**

| Term | Definition |
|---|---|
| **ADC** | Analog-to-Digital Converter |
| **AGC** | Automatic Gain Control |
| **AM** | Amplitude Modulation |
| **ASK** | Amplitude Shift Keying |
| **AUX** | Auxiliary |
| **BLF** | Backscatter Link Frequency / Backward Link Frequency |
| **BPF** | Band Pass Filter |
| **CW** | Continuous Wave (Pure sine wave transmitted by reader when listening to tags) |
| **DAC** | Digital-to-Analog Converter |
| **DRM** | Dense Reader Mode |
| **DSB** | Double Sideband |
| **EOT** | End of Transfer |
| **EPC** | Electronic Product Code |
| **FCC** | Federal Communications Commission (US Regulatory Body) |
| **FIFO** | First In, First Out |
| **FIR** | Finite Impulse Response |
| **I** | In-phase |
| **IF** | Intermediate Frequency |
| **IIP** | Input Intercept Point |
| **IIR** | Infinite Impulse Response |
| **I-Q** | In-phase Quadrature |
| **ISM** | Industrial, Science, and Medical |
| **ISO** | International Standards Organization |
| **ISO18000** | Tags and Readers conforming to ISO/IEC FDIS 18000-6:2003(E) |
| **LBT** | Listen Before Talk |
| **LFSR** | Linear Feedback Shift Registers |
| **LNA** | Low Noise Amplifier |
| **LO** | Local Oscillator |
| **LUT** | Lookup Table |
| **MSB** | Most Significant Bit |
| **PA** | Power Amplifier |
| **PER** | Packet Error Rate |
| **PLL** | Phase Locked Loop |
| **POR** | Power On Reset |
| **PR** | Phase Reversal |
| **Q** | Quadrature-phase |

| Term | Definition |
|---|---|
| **RAIN** | UHF Gen 2 RFID |
| **RF** | Radio Frequency |
| **RFID** | Radio Frequency Identification |
| **RSSI** | Received Signal Strength Indicator |
| **RX** | Receiver |
| **S11** | Input reflection coefficient S-parameter |
| **SJ** | Self Jammer — also known as Tx carrier present at the RX, typically from antenna reflection |
| **SJC** | Self Jammer Cancellation — circuitry that removes SJ from RX port |
| **SPI** | Serial Peripheral Interface |
| **TX** | Transmitter |
| **TCXO** | Temperature Compensated Crystal Oscillator |
| **UHF** | Ultra High Frequency (~900 MHz) |
| **VCO** | Voltage Controlled Oscillator |

# 9 REFERENCE DOCUMENTS

Related documents are listed in Table 30. All documents can be downloaded from the Impinj support portal here: https://support.impinj.com/hc/en-us/sections/360003305060

**Table 30: Reference Documents**

| Document | Description |
|---|---|
| **Impinj E910 and E710 Development Kit User's Guide** | Documents how to use the Impinj E910 and E710 development kits, Impinj reader chip SDK, and host examples, including Quick Start Guide. |
| **Impinj Reader Chip SDK Documentation** | Documents the interfaces between the host and the Impinj reader chips, including the SPI wireline, messages, registers, and FIFOs. |
| **Impinj E710 Development Board Application Note** | Documents the Impinj E710 development board hardware, circuit topologies, design performance, and potential modifications. |
| **Impinj Reader Chip Datasheet** **(this document)** | Documents the Impinj E910, E710, E510, and E310 reader chips, including electrical and mechanical specifications. |
| **Impinj Reader Chip Gen2X Inventory Application Note** | Documents how to use the Impinj Gen2X features with Impinj Reader Chips. |
| **Impinj Reader Chip RF Performance Optimization Application Note** | Documents how to measure and optimize RF performance in Impinj Reader Chip-based RAIN RFID reader devices. |
| **Impinj E910-, E710, E510, and E310-Based Reader Calibration Application Note** | Documents an example procedure and background to calibrate an Impinj reader chip-based RAIN RFID reader. |

# 10 DOCUMENT CHANGE LOG

**Table 31: Document Change Log**

| Version | Date | Description |
|---|---|---|
| **1.0** | 2021-05-27 | • First production version of this document. For details on preliminary changes, please contact support@impinj.com |

| Version | Date | Description |
|---|---|---|
| **1.1** | 2021-12-06 | • Added tag read rate to overview in Table 1<br>• Added section 2.4.9 - Host SPI Interface Functional Specifications<br><br>Updated RF modes and tag read rates for FW v1.1 in Table 1, **Error! Reference source not found.** and The E Family reader chips operate seamlessly across Gen2 and Gen2X inventory rounds using the reader modes detailed in Table 10 and Table 11 below. To initiate a Gen2 inventory round, the E Family reader chips send a Gen2 preamble followed by a *Query* command, and for a Gen2X inventory round, the E Family reader chip sends a Gen2X preamble followed by a *Scan* command. The reader controls whether subsequent inventory rounds are Gen2 or Gen2X by sending a *Query* or *Scan*, respectively. Supporting tag chips share session and select flag values across Gen2 and Gen2X inventory rounds, allowing seamless tag population management across Gen2 and Gen2X.<br><br>All other commands are the same between Gen2 and Gen2X, but the frame-syncs are different. Gen2 inventory rounds use a Gen2 frame-sync whereas Gen2X inventory rounds use a Gen2X frame-sync. When in a Gen2 inventory round, tag chips ignore commands with a Gen2X frame sync, and vice versa. All commands except *Query* and *Scan* are common between Gen2 and Gen2X inventory rounds – the only difference is the frame-sync.<br><br>For more details on Gen2X inventory rounds please request support through the Impinj Support Portal at support.impinj.com.<br><br>• Table 10<br>• Increased maximum power consumption specs in Table 8<br><br>10.1.1.1 Populated RSSI Accuracy and Phase Measurement Accuracy specs in Impinj Gen2X Power Delivery<br><br>Powerup waveform shaping and extended Tari values allow E Family readers to deliver more power to tags, improving tag sensitivity up to 2 dB in both Gen2 and Gen2X inventory rounds.<br><br>Power Boost is an improved reader powerup waveform that delivers up to 2 dB additional power to supporting tag chips during powerup initialization, when they most need it. This additional initialization power increases overall tag chip operating sensitivity by up to a commensurate 2 dB. Extended Tari values further increase available power during reader commands. Power Boost and extended Tari values are available in both Gen2 and Gen2X inventory rounds.<br><br>For more information on enabling Power Boost and extended Tari values with E Family reader chips, please request support through the Impinj Support Portal at support.impinj.com.<br><br>10.1.2 Radio Specifications<br><br>• Table 18<br>• Removed "TBD" TX Spurious Emissions spec from Table 21<br>• Populated Auxiliary ADC INL spec in Table 22<br>• Added part markings in section 7.2<br>• Added recommended reflow profile in section 7.4 |
| **1.2** | 2022-02-28 | • Added a note below Figure 24 to clarify dimensions of chips from all assembly vendors<br>• Updated Figure 25 and Table 27 to match markings from all assembly vendors |

| | | |
|---|---|---|
| **1.3** | 2022-06-27 | • Added Impinj E910 reader chip throughout datasheet<br>• Renamed Pin 29 to “STARTUP/DIGITAL_IO[6]” in Table 3<br>• Added section 2.2.1 - Digital IO Default Drive Modes<br>• Added internally regulated voltages to section 2.3 and Figure 4<br>Added new FW v1.2 reader mode 202 in The E Family reader chips operate seamlessly across Gen2 and Gen2X inventory rounds using the reader modes detailed in Table 10 and Table 11 below. To initiate a Gen2 inventory round, the E Family reader chips send a Gen2 preamble followed by a *Query* command, and for a Gen2X inventory round, the E Family reader chip sends a Gen2X preamble followed by a *Scan* command. The reader controls whether subsequent inventory rounds are Gen2 or Gen2X by sending a *Query* or *Scan*, respectively. Supporting tag chips share session and select flag values across Gen2 and Gen2X inventory rounds, allowing seamless tag population management across Gen2 and Gen2X.<br>All other commands are the same between Gen2 and Gen2X, but the frame-syncs are different. Gen2 inventory rounds use a Gen2 frame-sync whereas Gen2X inventory rounds use a Gen2X frame-sync. When in a Gen2 inventory round, tag chips ignore commands with a Gen2X frame sync, and vice versa. All commands except *Query* and *Scan* are common between Gen2 and Gen2X inventory rounds – the only difference is the frame-sync.<br>For more details on Gen2X inventory rounds please request support through the Impinj Support Portal at support.impinj.com.<br>• Table 10<br>Clarified that reader mode sensitivity specs in The E Family reader chips operate seamlessly across Gen2 and Gen2X inventory rounds using the reader modes detailed in Table 10 and Table 11 below. To initiate a Gen2 inventory round, the E Family reader chips send a Gen2 preamble followed by a *Query* command, and for a Gen2X inventory round, the E Family reader chip sends a Gen2X preamble followed by a *Scan* command. The reader controls whether subsequent inventory rounds are Gen2 or Gen2X by sending a *Query* or *Scan*, respectively. Supporting tag chips share session and select flag values across Gen2 and Gen2X inventory rounds, allowing seamless tag population management across Gen2 and Gen2X.<br>All other commands are the same between Gen2 and Gen2X, but the frame-syncs are different. Gen2 inventory rounds use a Gen2 frame-sync whereas Gen2X inventory rounds use a Gen2X frame-sync. When in a Gen2 inventory round, tag chips ignore commands with a Gen2X frame sync, and vice versa. All commands except *Query* and *Scan* are common between Gen2 and Gen2X inventory rounds – the only difference is the frame-sync.<br>For more details on Gen2X inventory rounds please request support through the Impinj Support Portal at support.impinj.com.<br>• Table 10 are at typical Gen2 parameter values<br>• Increased LO and RX Pin maximum operating power specs in Impinj Gen2X Power Delivery<br>Powerup waveform shaping and extended Tari values allow E Family readers to deliver more power to tags, improving tag sensitivity up to 2 dB in both Gen2 and Gen2X inventory rounds.<br>Power Boost is an improved reader powerup waveform that delivers up to 2 dB additional power to supporting tag chips during powerup initialization, when they most need it. This additional initialization power increases overall tag chip operating sensitivity by up to a commensurate 2 dB. Extended Tari values further increase available power during reader commands. Power |

| Version | Date | Description |
|---|---|---|
| | | Boost and extended Tari values are available in both Gen2 and Gen2X inventory rounds.<br><br>For more information on enabling Power Boost and extended Tari values with E Family reader chips, please request support through the Impinj Support Portal at support.impinj.com.<br><br>10.1.3 Radio Specifications<br><br>• Table 18<br>  ○ Impinj E710, E510, and E310 LO pin operating power spec increased to +18 dBm max<br>  ○ Impinj E710, E510, and E310 RX pin operating power spec increased to +11 dBm max<br>• Added more detailed drawings of recommended PCB footprint dimensions in section 7.3.1<br>• Clarifications throughout |
| **1.4** | 2023-08-24 | • SDK+FW v2.0 updates<br>  ○ Added new reader modes to Table 12: Impinj E Family Reader Mode Read Rate Performance<br>• Fixed a typo in section 2.3.1 about the READY_N condition for entering bootloader mode<br>• Clarified startup sequence in section 2.3.1<br>• Added SPI parameters in section 2.4.9<br>• Added additional thermal data to Table 7: Chip Operating Conditions<br>• Added reader mode list in The E Family reader chips operate seamlessly across Gen2 and Gen2X inventory rounds using the reader modes detailed in Table 10 and Table 11 below. To initiate a Gen2 inventory round, the E Family reader chips send a Gen2 preamble followed by a *Query* command, and for a Gen2X inventory round, the E Family reader chip sends a Gen2X preamble followed by a *Scan* command. The reader controls whether subsequent inventory rounds are Gen2 or Gen2X by sending a *Query* or *Scan*, respectively. Supporting tag chips share session and select flag values across Gen2 and Gen2X inventory rounds, allowing seamless tag population management across Gen2 and Gen2X.<br><br>All other commands are the same between Gen2 and Gen2X, but the frame-syncs are different. Gen2 inventory rounds use a Gen2 frame-sync whereas Gen2X inventory rounds use a Gen2X frame-sync. When in a Gen2 inventory round, tag chips ignore commands with a Gen2X frame sync, and vice versa. All commands except *Query* and *Scan* are common between Gen2 and Gen2X inventory rounds – the only difference is the frame-sync.<br><br>For more details on Gen2X inventory rounds please request support through the Impinj Support Portal at support.impinj.com.<br><br>• Table 10: RAIN Gen2 Inventory Round Reader Mode IDs and Parameters<br>• Re-worded RX sensitivity spec in Table 12: Impinj E Family Reader Mode Read Rate Performance |

| Version | Date | Description |
| --- | --- | --- |
| **2** | 2024-05-14 | • Clarified chip startup sequence in section 2.3.1<br>• Re-organized electrical specification subsection 2.4.3 into two subsections: 2.4.3 and **Error! Reference source not found.**<br>• Corrected RF pin HBM ESD rating to HBM Class 2 in Table 6<br>• Corrected RF and non-RF pin CDM ESD rating to CDM Class C0b in Table 6<br>• Increased chip Idle power consumption maximum values in Table 8<br>• Corrected some reader mode parameters in The E Family reader chips operate seamlessly across Gen2 and Gen2X inventory rounds using the reader modes detailed in Table 10 and Table 11 below. To initiate a Gen2 inventory round, the E Family reader chips send a Gen2 preamble followed by a *Query* command, and for a Gen2X inventory round, the E Family reader chip sends a Gen2X preamble followed by a *Scan* command. The reader controls whether subsequent inventory rounds are Gen2 or Gen2X by sending a *Query* or *Scan*, respectively. Supporting tag chips share session and select flag values across Gen2 and Gen2X inventory rounds, allowing seamless tag population management across Gen2 and Gen2X.<br><br>All other commands are the same between Gen2 and Gen2X, but the frame-syncs are different. Gen2 inventory rounds use a Gen2 frame-sync whereas Gen2X inventory rounds use a Gen2X frame-sync. When in a Gen2 inventory round, tag chips ignore commands with a Gen2X frame sync, and vice versa. All commands except *Query* and *Scan* are common between Gen2 and Gen2X inventory rounds – the only difference is the frame-sync.<br><br>For more details on Gen2X inventory rounds please request support through the Impinj Support Portal at support.impinj.com.<br><br>• Table 10<br>• Updated sensitivity specs and moved them from Table 12 to Table 14 through Table 17<br>• Updated (improved) calibrated RSSI accuracy in Impinj Gen2X Power Delivery<br><br>Powerup waveform shaping and extended Tari values allow E Family readers to deliver more power to tags, improving tag sensitivity up to 2 dB in both Gen2 and Gen2X inventory rounds.<br><br>Power Boost is an improved reader powerup waveform that delivers up to 2 dB additional power to supporting tag chips during powerup initialization, when they most need it. This additional initialization power increases overall tag chip operating sensitivity by up to a commensurate 2 dB. Extended Tari values further increase available power during reader commands. Power Boost and extended Tari values are available in both Gen2 and Gen2X inventory rounds.<br><br>For more information on enabling Power Boost and extended Tari values with E Family reader chips, please request support through the Impinj Support Portal at support.impinj.com.<br><br>10.1.4 Radio Specifications<br><br>• Table 18<br>• Clarified Tx output power regulatory compliant range spec in Table 19<br>• Updated Tx clock harmonic spurs spec in Table 21<br>• Improved Tx in-band spurious emissions spec in Table 21<br>• Updated Tx out-of-band spurious emissions spec in Table 21<br>• Added section 2.4.7 - Memory Functional Specifications<br>• Corrected reflow profile reference document number in section 7.4<br>• Updated to new single digit document version numbering scheme |

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| **3** | 2024-10-10 | • Clarified power mode transitions in section 2.3<br>Updated reader modes for FW v2.1 in The E Family reader chips operate seamlessly across Gen2 and Gen2X inventory rounds using the reader modes detailed in Table 10 and Table 11 below. To initiate a Gen2 inventory round, the E Family reader chips send a Gen2 preamble followed by a *Query* command, and for a Gen2X inventory round, the E Family reader chip sends a Gen2X preamble followed by a *Scan* command. The reader controls whether subsequent inventory rounds are Gen2 or Gen2X by sending a *Query* or *Scan*, respectively. Supporting tag chips share session and select flag values across Gen2 and Gen2X inventory rounds, allowing seamless tag population management across Gen2 and Gen2X.<br>All other commands are the same between Gen2 and Gen2X, but the frame-syncs are different. Gen2 inventory rounds use a Gen2 frame-sync whereas Gen2X inventory rounds use a Gen2X frame-sync. When in a Gen2 inventory round, tag chips ignore commands with a Gen2X frame sync, and vice versa. All commands except *Query* and *Scan* are common between Gen2 and Gen2X inventory rounds – the only difference is the frame-sync.<br>For more details on Gen2X inventory rounds please request support through the Impinj Support Portal at support.impinj.com.<br>• Table 10 through Table 17<br>• Updated reader mode read rates in Table 12<br>• Clarified baseband filter pin series resistance in section 3.2.4 |
| **4** | 2024-12-03 | • Updated Overview to include Impinj Gen2X details<br>• Added sections 1.1.2 - Impinj E Family Gen2X Performance Enhancements and 1.1.3 - Impinj E Family Gen2X Protection Enhancements<br>• Added section 2.4.4 - Gen2 and Gen2X Reader Modes and Performance Specifications |

# 11 NOTICES