Datasheet

IMPINJ MONZA® 4 SERIES

TAG CHIP DATASHEET

IPJ-W1510

IPJ-W1512

IPJ-W1513

IPJ-W1535

1 OVERVIEW

With the Impinj Monza® 4 series of tag chips, Impinj builds upon the field-proven Monza chip family—well-regarded in the industry as the most reliable, consistent, flexible, and fully UHF Gen2-compliant tag chips available. The Impinj Monza 4 family provides a variety of models to suit diverse applications, including unique RFID privacy, tag orientation insensitivity, competitive and consistent read/write performance, and memory options optimized for use in manufacturing and supply chain industries.

1.1 Features

- True3D™ antenna technology—patented, dual-differential antenna ports enable compact Omni-directional tags, improving item-level read reliability
- QT® chip technology—protects business sensitive data while assuring consumers of privacy
    - Private/Public data profiles—two different memory maps that enable tag owners to control exposure of data
    - Short-range option to prevent unauthorized access
- Inlay compatibility between all Impinj Monza 4 tag chips
- Available memory options to support large user-memory applications
- BlockPermalock Gen2 command adds flexibility in memory usage
- FastID™ mode enables 2x to 3x faster EPC+TID inventory for authentication and other TID-based applications
- TagFocus™ mode suppresses previously read tags to enable capture of more tags
- 96-bit Serialized TID with 48-bit Serial Number
- Superior read sensitivity of -19.5 dBm (single port operation) or -22 dBm (with True3D) with a single dipole tag.
- High performance write sensitivity of -16.7 dBm, with a single dipole tag, for unparalleled commissioning and bulk encoding reliability.
- Memory write speed of 3.4 ms for 32-bit writes enables 1200 tags/minute programming
- Extended temperature range (-40°C to +85°C) for performance under hard conditions
- Impinj's field-rewritable NVM (optimized for RFID) provides 100,000 cycle/50-year retention reliability
- EPCglobal and ISO 18000-63 compliant, Gen2 compliant

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2 INTRODUCTION

2.1 Scope

This datasheet defines the physical and logical specifications for Gen2-compliant Impinj Monza 4 tag silicon, a reader-talks-first, radio frequency identification (RFID) component operating in the UHF frequency range.

2.2 Reference Documents

The following reference documents were used to compile this datasheet:

- EPC™ Radio Frequency Identity Protocols Class-1 Generation-2 UHF RFID Protocol for Communications at 860 MHz – 960 MHz (Gen2 Specification)
    - The conventions used in the Gen2 Specification (normative references, terms and definitions, symbols, abbreviated terms, and notation) were adopted in the drafting of this Impinj Monza 4 Tag Chip Datasheet. Users of this datasheet should familiarize themselves with the Gen2 Specification.
- Impinj Monza Wafer Assembly Specification
- Impinj Monza Wafer Map Orientation
- GS1 EPC™ Tag Data Standards Specification
- EPCglobal “Interoperability Test System for EPC Compliant Class-1 Generation-2 UHF RFID Devices” v.1.2.4, August 4, 2006
    - Impinj Monza 4 tag chips are compliant with this Gen2 interoperability standard.

Consult these documents for more information about compliance standards and specifications.

3 FUNCTIONAL DESCRIPTION

The Impinj Monza 4 tag chip family fully supports all requirements of the Gen2 specification as well as many optional commands and features (see Section 3.5 below). In addition, the Impinj Monza 4 tag chip family introduces a number of enhancements over previous generation chips on the market:

- Superior sensitivity yields highly improved performance, read/write range/reliability, and write rate
- Impinj patented True3D™ antenna technology enables smaller, less expensive tags with better performance, and supports orientation insensitivity without compromised performance
- Impinj patented QT® chip technology provides additional options for data protection, giving the user the ability control access to business-sensitive data
- Increased memory size options and in some models, the ability to permanently lock individual blocks of memory provide added flexibility
- Custom, yet fully Gen2-compliant S1 flag refresh and EPC + TID backscatter modes add more capability for previously difficult tagging applications

3.1 True3D™ Antenna Technology Improves Performance

Impinj Monza 4 series tag chips have an architecture unlike any other chip on the market. With True3D antenna technology, two fully independent, differential inputs enable omni-directional antenna designs, eliminating orientation-related missed reads or blind spots. (See Section 4.1 for details about how to

connect to these inputs.) Orientation insensitivity is particularly important in item-level applications and in situations where handheld readers are the norm.

For item-level tags, variability in orientation can be too great to overcome easily. For example, in a retail apparel application, the variety of ways an RFID tag on a garment might lay with respect to a reader are endless: folded on a shelf, hanging on a rack, boxed in the backroom, crumpled on the floor in the changing room, etc. To expect this tag to always have a particular orientation that facilitates reading is not realistic. In such cases, true omni-directional tag designs are paramount to successful data capture.

With the Impinj Monza 4 tag chip architecture, this type of orientation indifference is possible. To illustrate the difference between conventional tag chips and the Impinj Monza 4 series, examining their read range responses is useful.

Figure 1 provides a read range response plot for a conventional Impinj Monza 4 single-port tag using a dipole antenna configuration, not utilizing True3D antenna technology. Any single port tag, even using the best chip and innovative antenna design, will have a deficiency somewhere in its pattern. While the tag depicted in Figure 1 has excellent broadside performance, there are certain angles where a tag is less visible to a reader.

With the previous generation Impinj Monza tag chip, clever antenna design that took advantage of its dual input structure helped to remove the blind spots, or nulls (see Figure 2) but came at the cost of a compromise in long-range performance.

Figure 3 provides a read range response pattern for a tag using an Impinj Monza 4 tag chip. Compare Figure 3 to Figure 2. Notice that the response patterns in the Monza 4-based tag (Figure 3) are close to circular—no angle has significantly lower sensitivity than any other. And at every angle, the read range has increased.

With Impinj Monza 4 tag chips and True3D antenna technology, users achieve orientation insensitivity as well as excellent performance.

Figure 1: Read Range for Impinj Monza 4-based, 95 x 8 mm Dipole Tag (Impinj Reference E41)

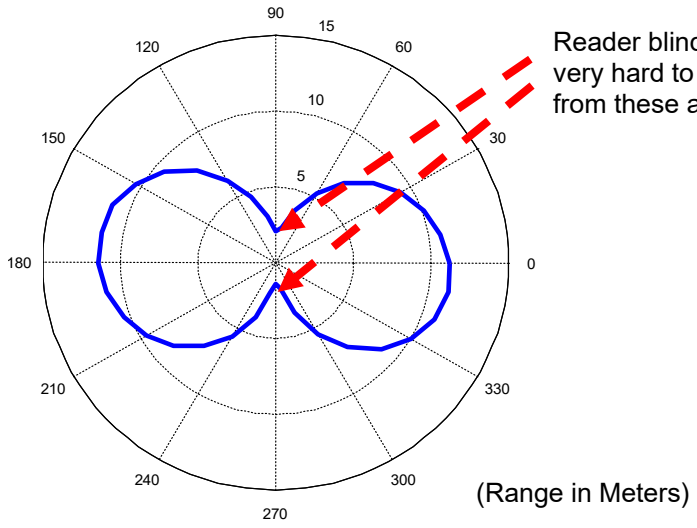
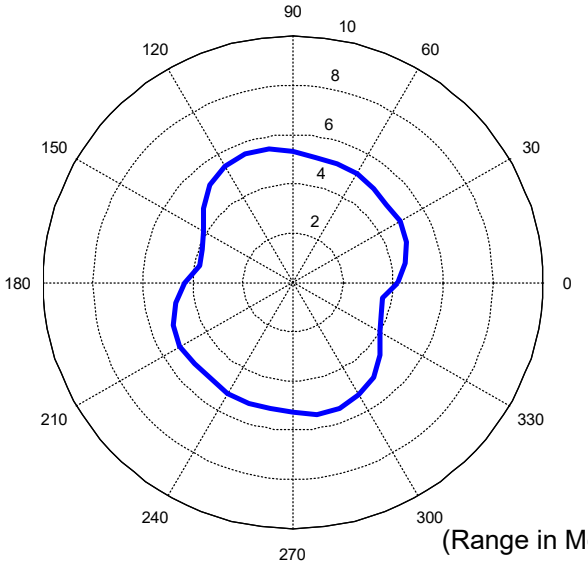


Figure 2: Read Range for Impinj Monza 3-Based, 46 mm2 Tag (Impinj Reference H32)



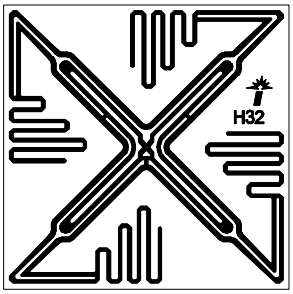
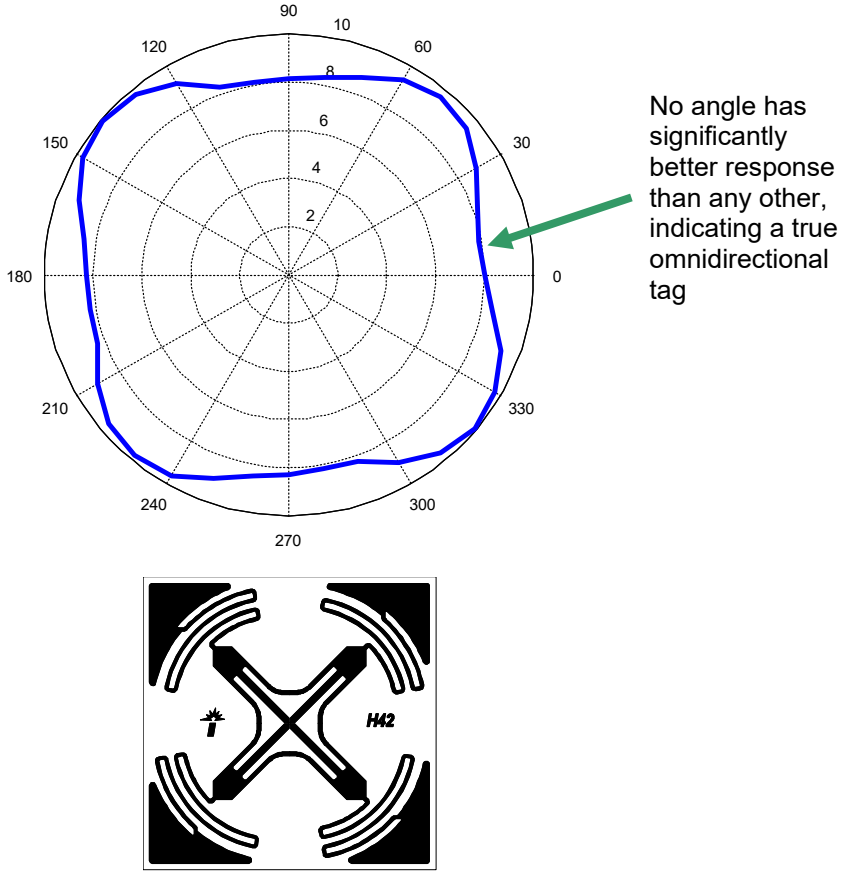


Figure 3: Read Range for Impinj Monza 4-Based, 46 mm2 Tag (Impinj Reference H42)



3.2 QT ® Chip Technology – Private, Public, Peek, and Short Range

Through QT chip technology, a tag owner/user can maintain two data profiles (one public, one private), allowing confidentiality of business-sensitive data while assuring consumers of privacy. The tag owner stores confidential data in the private data profile, which is protected by a password-controlled command and may only be accessed at very short read distances.

One example where such a feature would be useful is in a supply chain for luxury goods. The manufacturer may want to include information in the tag that would provide a guarantee of authenticity, record the time and place of manufacture for guarantee purposes, or include serial numbers.

After that item is packaged for distribution, however, such details might provide a security risk. If anyone possessing a reader can determine details about what is in a particular box, high-value goods could get diverted.

The Impinj Monza 4 tag chip's unique set of features helps to solve this problem.

3.2.1 Private/Public Profiles

The Private/Public profile capability, available in Impinj Monza 4QT tag chips, provides two memory configurations (i.e., profiles) in a single chip—one Private and one Public. An Impinj Monza 4QT chip only exposes a single profile at a time. The Private profile is the factory default setting. Figure 4 shows the chip's memory configuration when in the Private profile. The EPC memory typically contains an item serial number. The User memory might hold detailed information about the item. The TID memory, which

includes a 32-bit base TID, a 16-bit extended TID header, and a 48-bit serial number, uniquely identifies the Impinj Monza 4QT chip itself. Also included in TID memory is a 96-bit Public EPC, which is field-writeable by a user. In typical applications, the user writes a Public EPC value into this memory location then “publicizes” the tag. Although users are free to encode as little or as much information into this 96-bit Public EPC field as they chose (including no information at all), Impinj recommends certain usage guidelines to prevent these 96-bit Public EPCs from colliding with other tags. See section 3.2.5 for Impinj’s recommended usage guidelines.

At any point in the supply chain, for example at point-of-sale, users have the ability to switch QT tags to the Public profile. Figure 5 illustrates this profile. Once switched, the tag conceals its 128-bit EPC (EPC_Private), User Memory, 16-bit TID header, and 48-bit serial number. The tag exposes its Public EPC in EPC memory, remapped from its prior location in TID memory. When the tag is singulated, it sends this 96-bit public EPC. The only other information available to a reader is the 32-bit base TID. All other private memory contents appear non-existent to a reader reading the tag.

Figure 4: Impinj Monza 4QT Tag Chip Private Data Profile (Default)

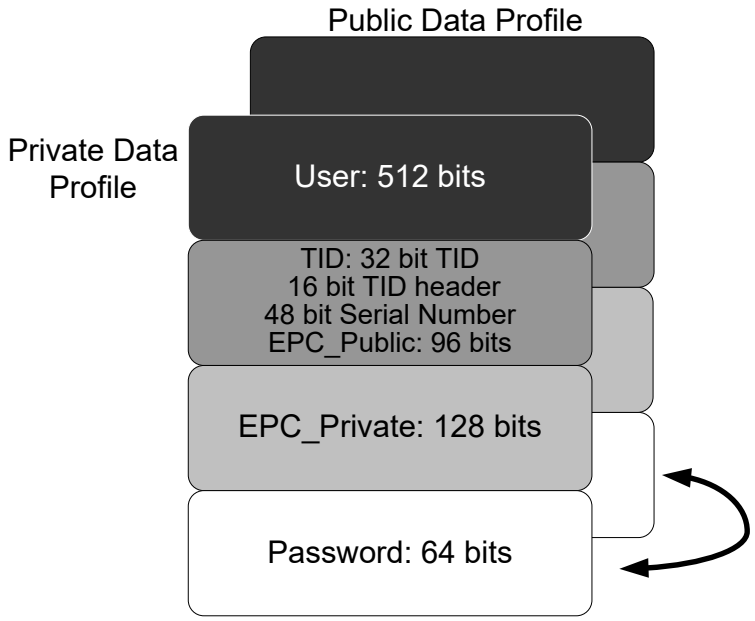
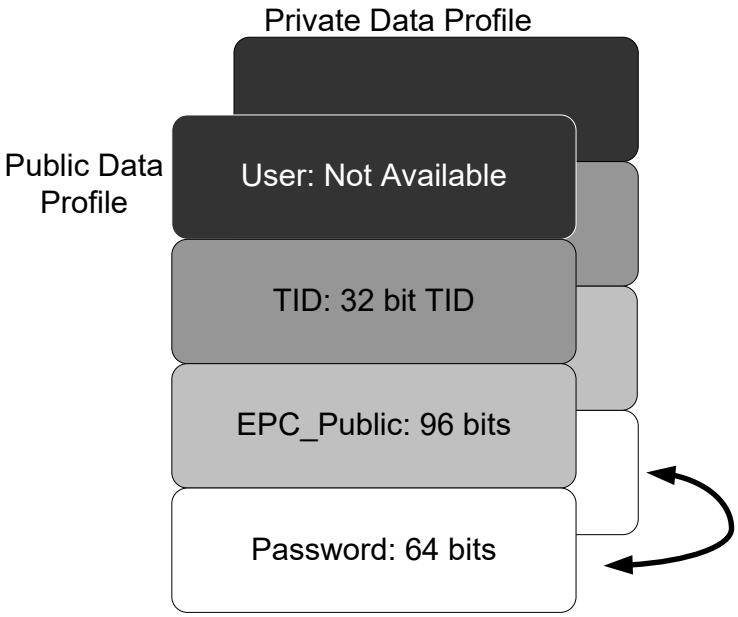


Figure 5: Impinj Monza 4QT Tag Chip Public Data Profile



The Private/Public profile features of the Impinj Monza 4QT tag chip are controlled by the QT command. Tags may be switched from Private profile to Public profile and back again, using the QT command. This QT command can be protected by a Short-Range Feature, by the tag's access password, or by both. See Section 3.2.2.

3.2.2 Public/Private Profile Protection

To secure the Private profile tag data, Impinj Monza 4QT chips offer a **Short-Range** feature. The Short-Range feature adds a layer of physical security by preventing readers farther than roughly one meter from the tag from switching the tag from Public to Private (or vice versa).

When Short-Range is enabled, the tag reduces its sensitivity in the OPEN and SECURED states by about 15 dB. The tag has normal sensitivity during singulation. However, before transitioning to the OPEN or SECURED states, the tag checks the RF power level—if it is above the short-range threshold then the tag will enter the OPEN or SECURED state, otherwise the tag will reset back to the READY state. The QT command is only available when a tag is in the SECURED state, so this power check effectively prevents the tag from accepting a QT command at long range.

A reader is always able to read a tag's currently exposed EPC (EPC_Public or EPC_Private, as appropriate for the current profile) at maximum range. However, when the Short-Range feature is enabled, a reader at long range that attempts to switch the tag's profile (for example, from Public to Private to read the tag's User memory) will see the tag lose power and drop out of its dialog with the reader. This short-range feature ensures that the information the tag's rightful owner wants to protect is not readable unless the tag is close to a reader antenna.

As a further layer of protection, the Access command defined in the Gen2 specification is fully operable for QT-enabled tags. If the tag's Access password is nonzero, a reader must provide this password before the tag will transition to the SECURED state. Because the QT command is only operable from the SECURED state, the Access password provides a secure mechanism against unauthorized readers issuing a QT command. In short, a QT tag can use physical protection (Short-Range), logical protection (Access password) or both to prevent unauthorized access.

The Short-Range feature is controlled by the QT command. (See Table 1 through Table 3.) The specific bit that controls the Short-Range mode is the QT_SR bit described in Table 3.

3.2.3 Peek

What would happen if a Public tag is switched to Private by an authorized user, for example to read User memory, and inadvertently left in the Private mode? In this situation, the tag could compromise its Private data. To help prevent this situation, Monza 4QT tag chips offer a **Peek** feature. With Peek, a reader can temporarily switch a Public tag to Private, access the Private information, then when the chip loses power it will automatically revert to its Public profile. Peek is controlled by the persistence bit in the QT command—to implement a Peek, set the Persistence bit to 0 in the QT command. See Table 2 for details.

3.2.4 QT Command Format

Table 1, Table 2, and Table 3 provide details about the custom Impinj QT command.

Table 1: QT Command Code

Command	Code	Length (Bits)	Details
QT	1110000000000000	68	• The QT command controls the switching of Impinj Monza 4QT between the Private and Public profiles • The tag must be in the SECURED state to transition to the memory indicated by the command • If a tag receives a QT command with an invalid handle, it ignores that command • The tag responds with the Insufficient Power error code if the power check fails on write • The tag responds with the Other error code if the write times out

Table 2: QT Command Details

QT Command	Code	Read/Write	Persistence	RFU	Payload	RN	CRC-16
#bits	16	1	1	2	16	16	16
Details	1110000000000000	0: Read 1: Write	0: Temporary 1: Permanent	00_b	QT Control	handle	

Table 3: QT Command Field Descriptions

<table>
<tr><th>Field</th><th>Description</th></tr>
<tr><td>Read/Write</td><td>• The Read/Write field indicates whether the tag reads or writes QT control data.
• Read/Write=0 means read the QT control bits in cache.
• Read/Write=1 means write the QT control bits</td></tr>
<tr><td>Persistence</td><td>• If Read/Write=1, the Persistence field indicates whether the QT control is written to nonvolatile (NVM) or volatile memory.
• Persistence=0 means write to volatile memory.
• Persistence=1 means write to NVM memory</td></tr>
<tr><td>RFU</td><td>• These bits are reserved for future use and will be ignored by Monza 4</td></tr>
<tr><td>Payload
(QT Control)</td><td>• This field controls the QT functionality. These bits are ignored when the Read/Write field equals 0.
• Bit 15 (MSB) is first transmitted bit of the payload field.
<table>
<tr><th>Bit #</th><th>Name</th><th>Description</th></tr>
<tr><td>15</td><td>QT_SR</td><td>1: Tag reduces range if in or about to be in OPEN or SECURED state
0: Tag does not reduce range</td></tr>
<tr><td>14</td><td>QT_MEM</td><td>1: Tag uses Public Memory Map (see Table 10)
0: Tag uses Private Memory Map (see Table 9)</td></tr>
<tr><td>13:0</td><td colspan="2">Reserved for future use. Tag will return these bits as zero.</td></tr>
</table></td></tr>
<tr><td>RN</td><td>• The tag will ignore any QT command received with an invalid handle</td></tr>
</table>

The tag response to the QT Command with Read/Write = 0 uses the preamble specified by the TRext value in the Query command that initiated the round. See Table 4 for read response details.

Table 4: Tag Response to QT Read Command

	Header	Data	RN	CRC-16
#bits	1	16	16	16
Description	0	QT Control	handle	

The tag response to the QT Command with Read/Write =1 uses the extended preamble. See Table 5 for write response details. Note that a reader should not presume that a tag has properly executed a QT Write command unless and until it receives the response shown in Table 5 from the tag.

Table 5: Tag Response to a Successful QT Write Command

	Header	RN	CRC-16
#bits	1	16	16
Description	0	handle	

3.2.5 Recommended Public EPC Usage Guidelines

The GS1 EPC Tag Data Standards specifies the general structure of the EPC data field (for the latest version of this standard, visit http://www.gs1.org/epc/tag-data-standard). If tag users wish to have the Public EPC hold information in any of the currently defined formats (e.g., SGTIN-96), they should follow this specification.

For any other use of this data field, tag users must take care not to create content that conflicts with the standard. For example, a retailer should not set the MSBs to "0011 0000" because that could be interpreted as an SGTIN-96-tagged item.

To create Public EPCs that do not conflict with already defined usage, Impinj recommends the following (see also Table 6):

- The first 8 bits of header should always be zero to avoid conflict with already standardized EPC formats.
- The next 32 bits should hold a Private Enterprise Number (PEN) (number obtainable from the Internet Assigned Numbers Authority (IANA) at http://pen.iana.org/pen/app) that uniquely identifies a company or organization. If tag users do not wish to have even this level of identification (i.e., they desire full privacy), the PEN should be set to all zeros.
- The last 56 bits hold data fields specified by each entity for their application.

Table 6: Recommended Format for Public EPC Contents

Header (00000000)	Private Enterprise Number (32 bits)	Data Fields (56 bits)

3.2.5.1 Example Public EPC Use Case – Retail Environment

After a sale, a retailer might conceal any proprietary information available in the EPC_Private memory by switching the tag to the Public profile. But they still need a means of verifying that a particular item came from their company to support return logistics. And to avoid consumer privacy concerns, any information entered into the EPC_Public memory must not be unique.

By setting up a format such as that shown in Table 7, the retailer has sufficient information to support returns, verify that the item came from their company, determine the type of return, and identify stolen merchandise without having such unique numbers that a consumer's privacy is at risk.

Note: This format is for illustration purposes only. Tag users should consult the EPC Tag Data Standard when designing their format to ensure compliance.

Table 7: Example EPC_Public Format – Retail Case

Header (8 Bits)	Pen (32 Bits)	Mode (8 Bits)	Store Number (16 Bits)	Date Code (32 Bits)	Comments
00h	0000 0000 h	00 h	0000 h	0000 0000 h	Full Privacy Mode
00h	0000 0192 h	01 h	000F h	00C1 F7DA h	Store Return
00h	0000 0192 h	02 h	000F h	00A1 07DA h	Store Return, Password Required
00h	0000 0192 h	03 h	000F h	FFFF FFFA h	Date Field Coded to Indicate that Item Was Not Sold

3.3 Increased Memory Options

Tag users have asked for increased memory in RFID tag chips, and the Impinj Monza 4 family offers a variety of options. See Table 8. For detailed memory maps, see Section 5.1. The extended User memory of the Impinj Monza 4QT supports applications where users cannot count on a database connection. The 512 bits of User memory enables a portable, but private database to travel with the tag. The Impinj Monza 4E, with extended EPC memory, enables compliance with regional and industry-segment mandates that require more than 96-bit EPC numbers, as well as provides a faster access form of memory. The industrial/automotive-focused Impinj Monza 4i offers capabilities to leverage data logging.

Table 8: Impinj Monza 4 Memory Options

Model	User Memory	EPC Memory	True3D Technology	Serialized TID	QT Technology
Monza 4QT	512	128*	✓	✓	✓
Monza 4E	128	496*	✓	✓	–
Monza 4D	32	128*	✓	✓	–
Monza 4i	480	256*	✓	✓	–

The EPC is factory encoded with 96 bits to ensure backward compatibility with older readers. Users must encode Impinj Monza 4 tag chips above 96 bits.

3.3.1 Extended User Memory Option

Impinj offers a version of the Impinj Monza 4, the Monza 4QT, with 512 bits of user memory, 128 bits of EPC memory, and a serialized TID. See Table 9.

In addition to the increased memory size, Impinj Monza 4QT tag chips offer the ability to independently lock four fixed, 128-bit sections of user memory (BlockPermalock). This feature is particularly useful for situations such as in a supply chain, where various participants along the chain may want to record data, but not necessarily have it be openly available to all parties.

Table 9: Impinj Monza 4QT (Private Mode) Memory Organization

Memory Section	Description
User	512 bits
TID (not changeable)	Serial Number – 48 bits
	Extended TID Header – 16 bits
	Company/Model Number – 32 bits
EPC_Public	96 bits
EPC_Private	128 bits
Passwords	Kill/Access – 64 bits

Table 10: Impinj Monza 4QT (Public Mode) Memory Organization

Memory Section	Description
TID (Not Changeable)	Company/Model Number – 32 bits
EPC_Public	96 bits
Passwords	Kill/Access – 64 bits

3.3.2 Extended EPC Memory Option

Because of the way the protocol works, data stored in user memory requires multiple steps to access. For situations where memory must be accessed with some degree of speed, a larger User memory may not meet access speed requirements. To provide larger memory with the type of throughput required by some applications as well as meet the needs of applications requiring greater than 96-bit EPC numbers, Impinj also offers a variant of the Monza 4 tag chip with increased EPC memory. See Table 11.

Table 11: Impinj Monza 4E Memory Organization

Memory Section	Description
User	128 bits
TID (not changeable)	Serial Number – 48 bits
	Extended TID Header – 16 bits
	Company/Model Number – 32 bits
EPC	496 bits
Passwords	Kill/Access – 64 bits

3.3.3 Basic Memory Option

For applications where large memory is not required, the Impinj Monza 4D offers the superior sensitivity, True3D™ antenna support and unique TID with a more standard memory size. See Table 12.

Table 12: Impinj Monza 4D Memory Organization

Memory Section	Description
User	32 bits
TID (not changeable)	Serial Number – 48 bits
	Extended TID Header – 16 bits
	Company/Model Number – 32 bits
EPC	128 bits
Passwords	Kill/Access – 64 bits

3.3.4 Industrial/Automotive Application Focused Option

The Impinj Monza 4i is specifically targeted for industrial applications that require a moderately sized EPC along with large amount of user memory. The Impinj Monza 4i tag chip offers capabilities to leverage data logging to track, monitor, timestamp, and record item maintenance, component status, and environmental conditions, ensuring the historical record of the item is factual and true.

Impinj Monza 4i is also ideal for automotive markets to track extended serial numbers such as a Vehicle Identification Number. It can be used effectively in the following two major usages for automotive applications:

- Manufacturing control: quality checks for vehicle parts in assembly line, data is written in every production step.
- Logistics for finished vehicles: check condition of car parts like gear boxes, bumpers, airbags, dashboards, etc.

The Impinj Monza 4i includes 480-bit User memory and 256-bit EPC memory and provides all the standard features of the Monza 4 family of tag chips. See Table 13. In addition, Impinj Monza 4i tag chips offer the ability to independently lock four fixed sections of user memory (BlockPermalock). This feature is particularly useful for situations such as in a supply chain, where various participants along the chain may want to record data, but not necessarily have it openly available to all parties.

Table 13: Impinj Monza 4i Memory Organization

Memory Section	Description
User	480 bits
TID (not changeable)	Serial Number – 48 bits
	Extended TID Header – 16 bits
	Company/Model Number – 32 bits
EPC	256 bits
Passwords	Kill/Access – 64 bits

3.4 Advanced Impinj Features Support More Effective Inventory

Impinj Monza tag chips support two patented features designed to boost inventory performance for traditional EPC and TID-based applications:

- TagFocus™ mode minimizes redundant reads of strong tags, allowing the reader to focus on weak tags that are typically the last to be found. Using TagFocus, readers can suppress previously read tags by indefinitely refreshing their S1 B state.
- FastID™ mode makes TID-based applications such as authentication practical by boosting TID-based inventory speeds by 2 to 3 times. Readers can inventory both the EPC and the TID without having to perform an access command. Setting the EPC word length to zero enables TID-only serialization. FastID is supported by all Impinj Monza 4 tag chips except for Monza 4E and Monza 4QT when in public mode.

3.5 Support for Optional Gen2 Commands

Impinj Monza 4 tag chips support the optional commands listed in Table 14.

Table 14: Supported Optional Gen2 Specification Commands

Command	Code	Length (Bits)	Details
Access	11000110	56	
BlockWrite	11000111	>57	• Accepts valid one-word commands • Accepts valid two-word commands if pointer is an even value • Returns error code (00000000_2) if it receives a valid two-word command with an odd value pointer • Returns error code (00000000_2) if it receives a command for more than two words • Does not respond to block write commands of zero words
BlockPermalock	11001001	>66	• User Memory in Impinj Monza 4QT (in Private mode) and Monza 4i only (see Table 15 and Table 16 for details) • Ignored by Impinj Monza 4E, Monza 4D, and Monza 4QT (in Public mode)

Table 15: Impinj Monza 4QT (Private mode) BlockPermalock blocks

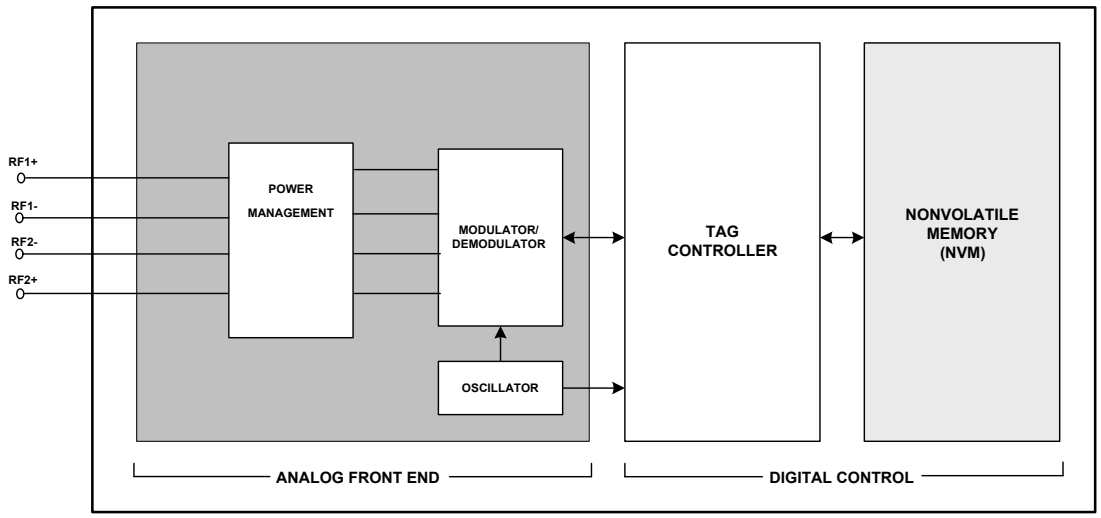
User Memory Bit Address Range	Blocks
384 - 511	BLOCK 3 (128 bits)
256 - 383	BLOCK 2 (128 bits)
128 - 255	BLOCK 1 (128 bits)
0 - 127	BLOCK 0 (128 bits)

Table 16: Impinj Monza 4i BlockPermalock blocks

User Memory Bit Address Range	Blocks
384 - 479	BLOCK 3 (96 bits)
256 - 383	BLOCK 2 (128 bits)
128 - 255	BLOCK 1 (128 bits)
0 - 127	BLOCK 0 (128 bits)

3.6 Impinj Monza 4 Tag Chip Block Diagram

Figure 6: Block Diagram



3.7 Pad Descriptions

Impinj Monza 4 tag chips have four external pads available to the user: RF1+, RF1-, RF2+, and RF2-, which are two fully independent, differential antenna ports (with one positive and one negative input pad each), as shown in Table 17 (see also Figure 6, and Figure 7). Note that none of these pads connects to the chip substrate.

Table 17: Pad Descriptions

External Signals	External Pad	Description
RF1+	1	Differential RF Input Pads for Antenna 1, which are isolated from the RF Input Pads for Antenna 2
RF1-	1	
RF2+	1	Differential RF Input Pads for Antenna 2, which are isolated from the RF Input Pads for Antenna 1
RF2-	1	

3.8 Dual Antenna Input

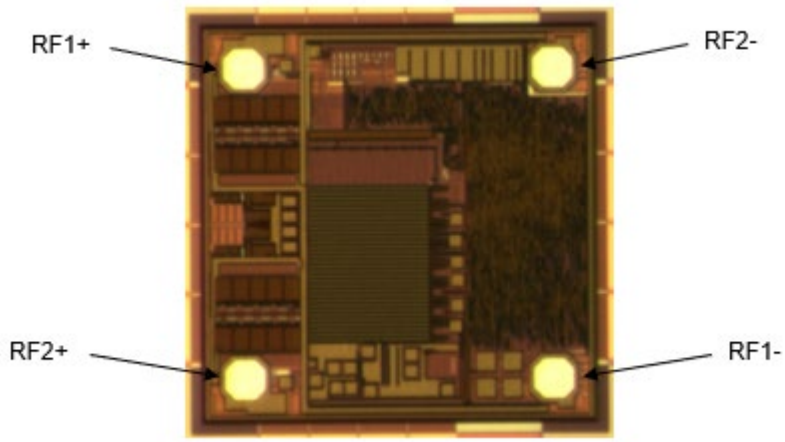
All interaction with Impinj Monza 4 series tag chips, including generation of its internal power, air interface, negotiation sequences, and command execution, occurs via its two differential antenna ports. The dual antenna ports enable antenna design diversity, which in turn minimizes a tag's orientation sensitivity, particularly when the two antennas are of different types (e.g., a combination of loop and

dipole) or are otherwise oriented on different axes (X-Y). The dual antenna port configuration also enables increased read and write ranges.

The two antenna ports operate independently. The power management circuitry receives power from the electromagnetic field induced in the pair, and the demodulator exploits the independent antenna connections, combining the two demodulated antenna signals for processing on-chip.

Impinj Monza 4 tag chips may also be configured to operate using a single antenna port by simply connecting just one of the two antenna ports. The unused port should be left to float.

Figure 7: Impinj Monza 4 Tag Chip Die Orientation



3.9 Impinj Monza 4 Antenna Reference Designs

All Impinj Monza 4 series tag chips (Monza 4QT, Monza 4E, Monza 4D and Monza 4i) are designed to be drop-in compatible for antenna inlay designs. Impinj has a set of reference designs available for use by Monza customers under terms of the Impinj Antenna License Agreement.

These reference designs are available here:

https://support.impinj.com/hc/en-us/sections/200454558-Monza-Reference-Design-Documents-Downloads

These documents are restricted. To gain access if these documents cannot be accessed, submit a request for access using the following link. Make sure to select the option “Monza Antenna Reference Designs”.

https://access.impinj.com/prtlaccessrequest

3.10 Impinj Monza 4 Tag Chip Dimensions

The Impinj Monza 4 features a 590 µm x 590 µm square die size.

3.11 Power Management

The tag is activated by proximity to an active reader. When the tag enters a reader’s RF field, the Power Management block converts the induced electromagnetic field to the DC voltage that powers the chip.

3.12 Modulator/Demodulator

The Impinj Monza 4 tag chip demodulates any of a reader's three possible modulation formats, DSB-ASK, SSB-ASK, or PR-ASK with PIE encoding. The tag communicates to a reader via backscatter of the incident RF waveform by switching the reflection coefficient of its antenna pair between reflective and

absorptive states. Backscattered data is encoded as either FM0 or Miller subcarrier modulation (with the reader commanding both the encoding choice and the data rate).

3.13 Tag Controller

The Tag Controller block is a finite state machine (digital logic) that carries out command sequences and also performs a number of overhead duties.

3.14 Nonvolatile Memory

Impinj Monza 4 tag chip embedded memory is nonvolatile memory (NVM) cell technology, specifically optimized for exceptionally high performance in RFID applications. All programming overhead circuitry is integrated on chip. Impinj Monza 4 series tag chip NVM provides 100,000 cycle endurance/50-year data retention.

The NVM block is organized into three segments:

- User memory (32, 128, 480, or 512 bits depending on model)
- EPC Memory (128, 256, or 496 bits, depending on model)
- Reserved Memory (which contains the Kill and Access passwords).

The ROM-based Tag Identification (TID) memory contains the EPCglobal class ID, the manufacturer identification, and the model number. For Impinj Monza 4 series tag chips, it also contains an extended TID consisting of a 16-bit header and 48-bit serialization.

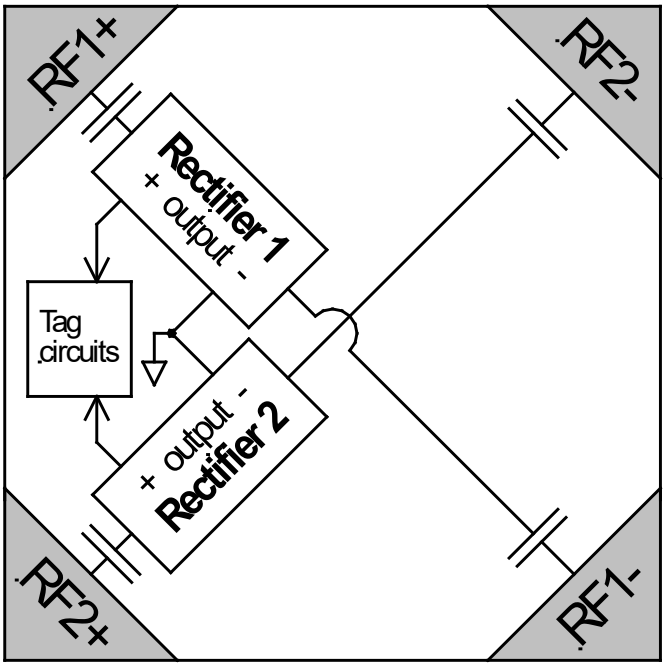
4 INTERFACE CHARACTERISTICS

This section describes the RF interface of the tag chip and the modulation characteristics of both communication links: reader-to-tag (Forward Link) and tag-to-reader (Reverse Link).

4.1 Making Connections

Impinj Monza 4 series tag chips take advantage of Impinj's patented rectifier technology to implement dual, independent ports. A port is defined between a pair of pads: the RF1+ and RF1- pair together forming Port 1 and the RF2+ and RF2- pair forming Port 2. A conceptual diagram of the RF front end is shown in Figure 8. The two ports have identical electrical properties. See Section 4.1.4 for the target source impedance recommended by Impinj for best operation.

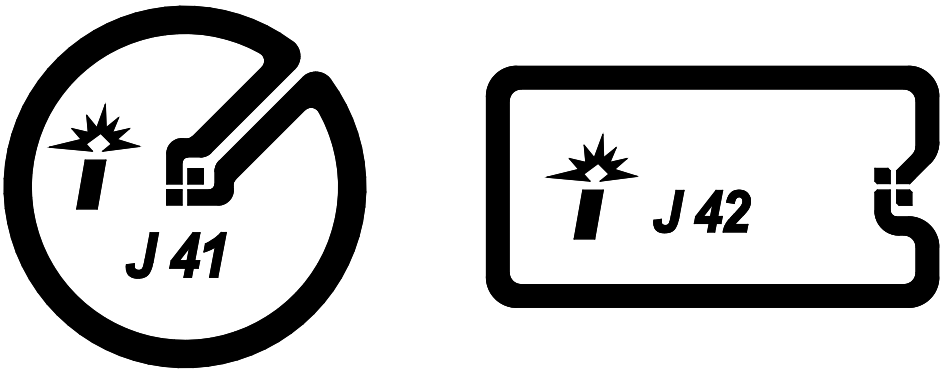
Figure 8: Conceptual model of dual independent ports



4.1.1 Single-port Connection Option

In the single-port configuration, the signal is applied to just one of the Impinj Monza 4 tag chip antenna ports. The antenna connects to a diagonal pair of pads and the remaining, unused pads are electrically isolated from the active traces. Figure 9 shows two examples of Impinj near-field antennas (Button and Blade) designed for connection in this fashion. The single-port configuration is common for near-field tag antennas and for very small or very thin antennas. It is not possible, however, to achieve true orientation insensitivity with a single port.

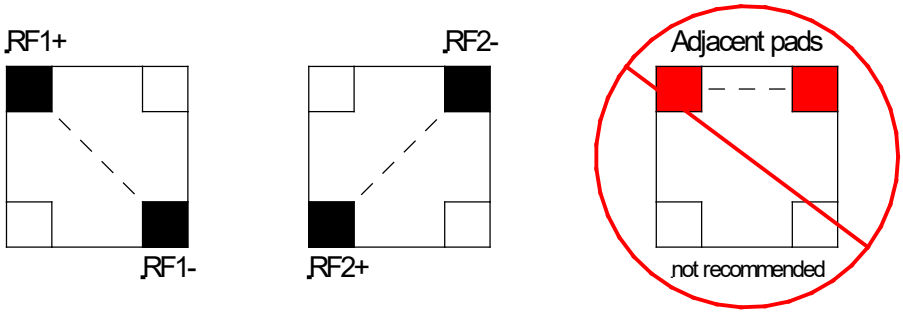
Figure 9: Antennas designed for a single-port connection. Button antenna (Left) and Blade antenna (Right), with antenna trace connections to diagonal pads of Impinj Monza 4.



The single-port configuration allows the chip to be mounted to the antenna at any 90-degree increment of rotation, as all four possible placements produce a valid connection between the antenna terminals and one of the Impinj Monza 4 ports. Because the two ports are electrically identical, there is no preferred orientation. The valid connections are shown in Figure 10, where the pad locations filled in black are those that are connected to the antenna traces. The dashed lines represent the electrical connections

within the chip. For contrast, the figure also illustrates an adjacent pad connection, which is acceptable for some Impinj tag chips but not for Impinj Monza 4.

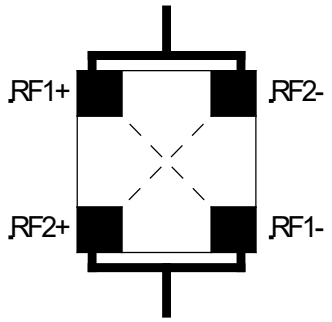
Figure 10: Chip/antenna connection possibilities for single-port configuration



4.1.2 Shunted-port Connection Option

In some rare circumstances, the antenna designer may find benefit in having a higher input capacitance. One example is in the design of very small, near-field antennas. The standard single-port connection presents a capacitance that resonates with a loop of approximately 12 mm diameter in a near-field tag such as the Button. If an application calls for a smaller tag, it is possible to employ the shunted-port connection to increase the input capacitance and reduce the loop size. This configuration, illustrated in Figure 11, energizes both ports simultaneously and loads the antenna with approximately twice the capacitance of a single port. A conductor loop with a diameter of about 7 to 8 mm is resonant with the shunted-port capacitance. This configuration incurs a slight (0.5 dB) efficiency penalty with corresponding loss in sensitivity compared to the single-port configuration, so it should be reserved for situations that mandate a very small tag.

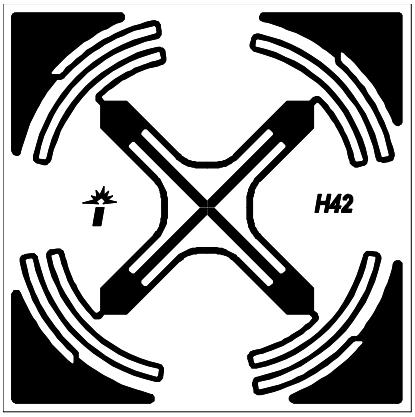
Figure 11: Chip/antenna connection for shunted-port configuration



4.1.3 Dual-port Connection Option

The advanced capabilities of Impinj Monza 4 really shine with a dual-port connection. This configuration is the focus of the True3D™ antenna technology that enables high-readability, orientation-insensitive tags. One of the fundamental principles for achieving such high levels of performance is symmetry by design. Impinj Monza 4 ports have an inherent electrical symmetry along both diagonal axes of the chip. A good antenna that extends that symmetry out to a larger geometry and into its resonant modes is ideal for realizing True3D™. An example of geometry that exhibits symmetry by design is shown in Figure 12.

Figure 12: Antenna design for dual-port connection. The geometry is formed by rotating and copying a one-quadrant "primitive," resulting in rotational symmetry.



4.1.4 Source Impedance

Table 18 shows the chip port impedances for Impinj Monza 4 tag chips across center frequencies of the primary regions of operation (North America, Europe, and Japan) for the single port configuration.

Table 18: Chip Port Impedances

Parameters		Typical Value	Comments
Intrinsic Capacitance*		1000 fF	Measured on bare die between pads RF1+ and RF1-, or between pads RF2+ and RF2-
Single-port connection			
Chip Load Model		1650 Ω || 1.21 pF	Linearized model of chip port, including typical mounting capacitance
Conjugate Match Impedance	866 MHz	13 + j151 Ω	Complex conjugate of Chip Load Model at specified frequency, expressed as an impedance
	915 MHz	11 + j143 Ω	
	956 MHz	10 + j137 Ω	
Read Sensitivity		-17.4 dBm	Measured at 25 °C; R=>T link using DSB-ASK modulation with 90% modulation depth, Tari=25 µs, and a T=>R link operating at 256 kbps with Miller M=4 encoding.
Write Sensitivity		-14.6 dBm	
Shunted-port connection			
Chip Load Model		1000 Ω || 2.48 pF	Linearized model of chip port, including typical mounting capacitance
Conjugate Match Impedance	866 MHz	5.5 + j74 Ω	Complex conjugate of Chip Load Model at specified frequency, expressed as impedance. For near field-only tag, disregard real component.
	915 MHz	4.9 + j70 Ω	
	956 MHz	4.5 + j67 Ω	
Read Sensitivity		-16.9 dBm	Measured at 25 °C; R=>T link using DSB-ASK modulation with 90% modulation depth, Tari=25 µs, and a T=>R link operating at 256 kbps with Miller M=4 encoding
Write Sensitivity		-14.1 dBm	
Dual-port connection			
Chip Load Model		1800 Ω || 1.21 pF	Ports act independently, so each port of a dual-port tag has the same impedance parameters as a single-port tag
Read Sensitivity		-19.9 dBm	Power incident at each port under conditions of equal power, arbitrary phase relation between signals
Write Sensitivity		-17.1 dBm	

*** Value does not include parasitic capacitance resulting from mounting the chip onto an antenna trace. Mounting capacitance is dependent on assembly parameters and manufacturing tolerance—users should evaluate and determine the appropriate mounting capacitance for their given process.**

4.2 Reader-to-Tag (Forward Link) Signal Characteristics

Table 19: Forward Link Signal Parameters

Parameter	Minimum	Typical	Maximum	Units	Comments
RF Characteristics					
Carrier Frequency	860		960	MHz	North America: 902–928 MHz Europe: 865–868 MHz
Maximum RF Field Strength			+20	dBm	Received by a tag with dipole antenna while sitting on a maximum power reader antenna
Short Range Sensitivity		6.0		dBm	
Tag Velocity During Write			4.5	Meters /sec	
Modulation Characteristics					
Modulation		DSB-ASK, SSB-ASK, or PR-ASK			Double and single sideband amplitude shift keying, and phase-reversal amplitude shift keying
Data Encoding		PIE			Pulse-interval encoding
Modulation Depth **(A-B)/A**	80		100	%	
Ripple, Peak-to-Peak **M_h=M_l**			5	%	Portion of A-B
Rise Time (tr,10-90%)	0		0.33 Tari	sec	
Fall Time (tf,10-90%)	0		0.33 Tari	sec	
Tari*	6.25		25	µs	Data 0 symbol period
PIE Symbol Ratio	1.5:1		2:1		Data 1 symbol duration relative to Data 0
Duty Cycle	48		82.3	%	Ratio of data symbol high time to total symbol time
Pulse Width	MAX (0.265Tari,2)		0.525Tari	µs	Pulse width defined as the low modulation time (50% amplitude)

*** Values are nominal minimum and nominal maximum, and do not include frequency tolerance. Apply appropriate frequency tolerance to arrive at absolute durations and frequencies.**

4.3 Reverse Link Signal Characteristics

Table 20: Reverse Link Signal Parameters

Parameter	Minimum	Typical	Maximum	Units	Comments
Modulation Characteristics					
Modulation		ASK			FET Modulator
Data Encoding		Baseband FM0 or Miller Subcarrier			
Change in Modulator Reflection Coefficient |ΔΓ|due to Modulation		0.8			$\|\Gamma\Delta\| - \left\|\Gamma_{reflect} - \Gamma_{absorb}\right\|$ (per read/write sensitivity, Table 19: Forward Link Signal Parameters)
Duty Cycle	45	50	55	%	
Symbol Period*	1.5625		25	µs	Baseband FM0
	3.125		200	µs	Miller-modulated subcarrier
Miller Subcarrier Frequency*	40		640	kHz	

*** Values are nominal minimum and nominal maximum, and do not include frequency tolerance. Apply appropriate frequency tolerance to arrive at absolute durations and frequencies.**

5 TAG MEMORY

5.1 Impinj Monza 4 Tag Chip Memory Maps

Table 21 through Table 25 describe the memory maps for Impinj Monza 4QT (both the Private and Public modes), Monza 4E, Monza 4D, and Monza 4i.

Table 21: Physical/Logical Memory Map – Impinj Monza 4QT (Private Mode)

Memory Bank Number	Memory Bank Name	Memory Bank Bit Address	Bit Number															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
11_2	User (NVM)	$1F0_h$-$1FF_h$	**User[15:0]**															
		$1E0_h$-$1EF_h$	**User[31:16]**															
		…	**…**															
		10_h-$1F_h$	**User[495:480]**															
		00_h-$0F_h$	**User[511:496]**															
10_2	EPC_Public (NVM)	$B0_h$-BF_h	**EPC_Public [15:0]**															
		$A0_h$-AF_h	**EPC_Public [31:16]**															
		90_h-$9F_h$	**EPC_Public [47:32]**															
		80_h-$8F_h$	**EPC_Public [63:48]**															
		70_h-$7F_h$	**EPC_Public [79:64]**															
		60_h-$6F_h$	**EPC_Public [95:80]**															
	TID (ROM)	50_h-$5F_h$	**TID_Serial[15:0]**															
		40_h-$4F_h$	**TID_Serial[31:16]**															
		30_h-$3F_h$	**TID_Serial[47:32]**															
		20_h-$2F_h$	**Extended TID Header**															
		10_h-$1F_h$	**Manufacturer ID**				**Model Number**											
		00_h-$0F_h$	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**	**Manufacturer ID**							
01_2	EPC_Private (NVM)	90_h-$9F_h$	**EPC_Private[15:0]**															
		80_h-$8F_h$	**EPC_Private [31:16]**															
		70_h-$7F_h$	**EPC_Private [47:32]**															
		60_h-$6F_h$	**EPC_Private [63:48]**															
		50_h-$5F_h$	**EPC_Private [79:64]**															
		40_h-$4F_h$	**EPC_Private [95:80]**															
		30_h-$3F_h$	**EPC_Private [111:96]**															
		20_h-$2F_h$	**EPC_Private [127:112]**															
		10_h-$1F_h$	**Protocol-Control Bits (PC)**															
		00_h-$0F_h$	**CRC-16**															
00_2	RESERVED (NVM)	30_h-$3F_h$	**Access Password[15:0]**															
		20_h-$2F_h$	**Access Password[31:16]**															
		10_h-$1F_h$	**Kill Password[15:0]**															
		00_h-$0F_h$	**Kill Password[31:16]**															

Table 22: Physical/Logical Memory Map – Impinj Monza 4QT (Public Mode)

Memory Bank Number	Memory Bank Name	Memory Bank Bit Address	Bit Number															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		10_h-$1F_h$	**Manufacturer ID**				**Model Number**											
		00_h-$0F_h$	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**	**Manufacturer ID**							
01_2	EPC_Public (NVM / Write Locked)	70_h-$7F_h$	**EPC_Public [15:0]**															
		60_h-$6F_h$	**EPC_Public [31:16]**															
		50_h-$5F_h$	**EPC_Public [47:32]**															
		40_h-$4F_h$	**EPC_Public [63:48]**															
		30_h-$3F_h$	**EPC_Public [79:64]**															
		20_h-$2F_h$	**EPC_Public [95:80]**															
		10_h-$1F_h$	**Protocol-Control Bits (PC)**															
		00_h-$0F_h$	**CRC-16**															
00_2	RESERVED (NVM / R/W Locked)	30_h-$3F_h$	**Access Password[15:0]**															
		20_h-$2F_h$	**Access Password[31:16]**															
		10_h-$1F_h$	**Kill Password[15:0]**															
		00_h-$0F_h$	**Kill Password[31:16]**															

Table 23: Physical/Logical Memory Map – Impinj Monza 4E

Memory Bank Number	Memory Bank Name	Memory Bank Bit Address	Bit Number															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
11_2	User (NVM)	70_h-$7F_h$	**User[15:0]**															
		60_h-$6F_h$	**User[31:16]**															
		…	**…**															
		10_h-$1F_h$	**User[111:96]**															
		00_h-$0F_h$	**User[127:112]**															
10_2	TID (ROM)	50_h-$5F_h$	**TID_Serial[15:0]**															
		40_h-$4F_h$	**TID_Serial[31:16]**															
		30_h-$3F_h$	**TID_Serial[47:32]**															
		20_h-$2F_h$	**Extended TID Header**															
		10_h-$1F_h$	**Manufacturer ID**				**Model Number**											
		00_h-$0F_h$	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**	**Manufacturer ID**							
01_2	EPC (NVM)	200_h-$20F_h$	**EPC[15:0]**															
		$1F0_h$-$1FF_h$	**EPC[31:16]**															
		$1E0_h$-$1EF_h$	**EPC[47:32]**															
		$1D0_h$-$1DF_h$	**EPC[63:48]**															
		…	**…**															
		40_h-$4F_h$	**EPC[463:448]**															
		30_h-$3F_h$	**EPC[479:464]**															
		20_h-$2F_h$	**EPC[495:480]**															
		10_h-$1F_h$	**Protocol-Control Bits (PC)**															
		00_h-$0F_h$	**CRC-16**															
00_2	RESERVED (NVM)	30_h-$3F_h$	**Access Password[15:0]**															
		20_h-$2F_h$	**Access Password[31:16]**															
		10_h-$1F_h$	**Kill Password[15:0]**															
		00_h-$0F_h$	**Kill Password[31:16]**															

Table 24: Physical/Logical Memory Map – Impinj Monza 4D

Memory Bank Number	Memory Bank Name	Memory Bank Bit Address	Bit Number															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
11_2	User (NVM)	10_h-$1F_h$	**User[15:0]**															
		00_h-$0F_h$	**User[31:16]**															
10_2	TID (ROM)	50_h-$5F_h$	**TID_Serial[15:0]**															
		40_h-$4F_h$	**TID_Serial[31:16]**															
		30_h-$3F_h$	**TID_Serial[47:32]**															
		20_h-$2F_h$	**Extended TID Header**															
		10_h-$1F_h$	**Manufacturer ID**				**Model Number**											
		00_h-$0F_h$	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**	**Manufacturer ID**							
01_2	EPC (NVM)	90_h-$9F_h$	**EPC[15:0]**															
		80_h-$8F_h$	**EPC[31:16]**															
		70_h-$7F_h$	**EPC[47:32]**															
		60_h-$6F_h$	**EPC[63:48]**															
		50_h-$5F_h$	**EPC[79:64]**															
		40_h-$4F_h$	**EPC[95:80]**															
		30_h-$3F_h$	**EPC[111:96]**															
		20_h-$2F_h$	**EPC[127:112]**															
		10_h-$1F_h$	**Protocol-Control Bits (PC)**															
		00_h-$0F_h$	**CRC-16**															
00_2	RESERVED (NVM)	30_h-$3F_h$	**Access Password[15:0]**															
		20_h-$2F_h$	**Access Password[31:16]**															
		10_h-$1F_h$	**Kill Password[15:0]**															
		00_h-$0F_h$	**Kill Password[31:16]**															

Table 25: Physical/Logical Memory Map – Impinj Monza 4i

Memory Bank Number	Memory Bank Name	Memory Bank Bit Address	Bit Number															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
11_2	User (NVM)	1D0h-1DFh	**User[15:0]**															
		1C0h-1CFh	**User[31:16]**															
		…	**…**															
		10h-1Fh	**User[463:448]**															
		00h-0Fh	**User[479:464]**															
10_2	TID (ROM)	50_h-$5F_h$	**TID_Serial[15:0]**															
		40_h-$4F_h$	**TID_Serial[31:16]**															
		30_h-$3F_h$	**TID_Serial[47:32]**															
		20_h-$2F_h$	**Extended TID Header**															
		10_h-$1F_h$	**Manufacturer ID**				**Model Number**											
		00_h-$0F_h$	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**	**Manufacturer ID**							
01_2	EPC (NVM)	200_h-$20F_h$	**EPC[15:0]**															
		$1F0_h$-$1FF_h$	**EPC[31:16]**															
		$1E0_h$-$1EF_h$	**EPC[47:32]**															
		$1D0_h$-$1DF_h$	**EPC[63:48]**															
		…	**…**															
		40_h-$4F_h$	**EPC[463:448]**															
		30_h-$3F_h$	**EPC[479:464]**															
		20_h-$2F_h$	**EPC[495:480]**															
		10_h-$1F_h$	**Protocol-Control Bits (PC)**															
		00_h-$0F_h$	**CRC-16**															
00_2	RESERVED (NVM)	30_h-$3F_h$	**Access Password[15:0]**															
		20_h-$2F_h$	**Access Password[31:16]**															
		10_h-$1F_h$	**Kill Password[15:0]**															
		00_h-$0F_h$	**Kill Password[31:16]**															

5.2 Logical vs. Physical Bit Identification

For the purposes of distinguishing most significant from least significant bits, a logical representation is used in this datasheet where MSBs correspond to large bit numbers and LSBs to small bit numbers. For example, Bit 15 is the logical MSB of a memory row in the memory map. Bit 0 is the LSB. A multi-bit word represented by WORD[N:0] is interpreted as MSB first when read from left to right. This convention

should not be confused with the physical bit address indicated by the rows and column addresses in the memory map; the physical bit address describes the addressing used to access the memory.

5.3 Memory Banks

Described in the following sections are the contents of the NVM and ROM memory, and the parameters for their associated bit settings.

5.3.1 Reserved Memory

Reserved Memory contains the *Access* and *Kill* passwords.

5.3.2 Passwords

Impinj Monza 4 tag chips have a 32-bit Access Password and 32-bit Kill Password. The default password for both Kill and Access is 00000000_h.

5.3.2.1 Access Password

The Access Password is a 32-bit value stored in Reserved Memory 20_h to $3F_h$ MSB first. The default value is all zeroes. Tags with a non-zero Access Password will require a reader to issue this password before transitioning to the secured state.

5.3.2.2 Kill Password

The Kill Password is a 32-bit value stored in Reserve Memory 00_h to $1F_h$, MSB first. The default value is all zeroes. A reader shall use a tag's kill password once to kill the tag and render it silent thereafter. A tag will not execute a kill operation if its Kill Password is all zeroes.

5.3.3 EPC Memory (EPC data, Protocol Control Bits, and CRC16)

As per the Gen2 specification, EPC memory contains a 16-bit cyclic-redundancy check word (CRC16) at memory addresses 00_h to $0F_h$, the 16 protocol-control bits (PC) at memory addresses 10_h to $1F_h$, and an EPC value beginning at address 20_h.

The protocol control fields include a five-bit EPC length, a one-bit user-memory indicator (UMI), a one-bit extended protocol control indicator, and a nine-bit numbering system identifier (NSI). The UMI bit is set to a default value of 1 to indicate presence of user memory bank. Only for Impinj Monza 4QT tag chip models, the UMI bit value will change to 0 automatically when it is configured to Public Mode, indicating no user memory. The default protocol control value is 3400_h. For Impinj Monza 4QT in Public Mode, the default value is 3000_h.

The tag calculates the CRC16 upon power-up over the stored PC bits and the EPC specified by the EPC length field in the stored PC. For more details about the PC field or the CRC16, see the Gen2 specification.

A reader accesses EPC memory by setting MemBank = 01_2 in the appropriate command and providing a memory address using the extensible-bit-vector (EBV) format. The CRC-16, PC, and EPC are stored MSB first (i.e., the EPC's MSB is stored in location 20_h).

For Impinj Monza 4QT tag chip models, the EPC memory contains a 96-bit, write-locked EPC in the Public mode, and a 128-bit EPC in the Private mode. For Impinj Monza 4QT chips (IPJ-W1502), the EPC value listed below is for the Private profile only.

The EPC written at time of manufacture is as shown in Table 26.

Table 26: EPC at Manufacture

Impinj Part Number	Protocol-Control Bits at Memory Addresses 10_h to $1F_h$[1]	EPC Value Pre-programmed at Manufacture (hex)[2]
IPJ-W1510 **IPJ-W1512** **IPJ-W1513** **IPJ-W1535**	0011 0100 0000 0000	3008 33B2 DDD9 0140 0000 0000

Note 1: The protocol-control bits for Impinj Monza 4QT in Public Mode are "0011 0000 0000 0000"

Note 2: The EPC is factory encoded with 96 bits to ensure backward compatibility with older readers. Users must encode Impinj Monza 4 tag chips above 96 bits.

5.3.4 Tag Identification (TID) Memory

The ROM-based Tag Identification memory contains Impinj-specific data. The bit locations in TID row 00_h-$0F_h$ store the EPCglobal™ Class ID (0xE2). The Impinj MDID (Manufacturer Identifier) for Impinj Monza 4 series tag chips is 100000000001 (the location of the manufacturer ID is shown in the memory map tables in Section 5.1). Note that a logic 1 in the most significant bit of the manufacturer ID (as in the example bordered in solid black in the table) indicates the presence of an extended TID consisting of a 16-bit header and a 48-bit serialization. The Impinj Monza 4 tag chip model number is located in TID memory row 10_h-$1F_h$ as shown in Table 27. See Table 28 for a list of the Impinj Monza 4 model numbers.

Table 27: TID Memory Details

Memory Bank Description	Memory Bank Bit Address	Bit Number															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
10_2 TID (ROM)	50_h-$5F_h$	**TID_Serial[15:0]**															
	40_h-$4F_h$	**TID_Serial[31:16]**															
	30_h-$3F_h$	**TID_Serial[47:32]**															
	20_h-$2F_h$	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
	10_h-$1F_h$	**0**	**0**	**0**	**1**	**Model Number (See Table 28)**											
	00_h-$0F_h$	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Table 28: Impinj Monza 4 Model Numbers

Model	Model Number
Impinj Monza 4QT	000100000101
Impinj Monza 4E	000100001100
Impinj Monza 4D	000100000000
Impinj Monza 4i	000100010100

6 ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed in this section may cause permanent damage to the tag. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this datasheet is not guaranteed or implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6.1 Temperature

Several different temperature ranges will apply over unique operating and survival conditions. Table 29 lists the ranges that will be referred to in this specification. Tag functional and performance requirements are met over the operating range, unless otherwise specified.

Table 29: Temperature Parameters

Parameter	Minimum	Typical	Maximum	Units	Comments
Extended Operating Temperature	-40		+85	°C	Default range for all functional and performance requirements
Storage Temperature	-40		+85/125	°C	At 125°C data retention is 1 year.
Assembly Survival Temperature			+260	°C	Applied for one minute
Temperature Rate of Change			4	°C / sec	During operation

6.2 Electrostatic Discharge (ESD) Tolerance

Table 30: ESD Limits

Parameter	Minimum	Typical	Maximum	Units	Comments
ESD			2,000	V	HBM (Human Body Model)

6.3 NVM Use Model

Tag memory is designed to endure 100,000 write cycles or retain data for 50 years.

7 ORDERING INFORMATION

Contact sales@impinj.com for ordering support.

Table 31: Ordering Information

Part Number	Product	Form	Processing Flow
IPJ-W1510-E00	Impinj Monza 4E tag chip	Wafer	Bumped, thinned (to ~100 µm) and diced
IPJ-W1510-F00	Impinj Monza 4E tag chip – alternate manufacturing location		
IPJ-W1512-E00	Impinj Monza 4QT tag chip		
IPJ-W1512-F00	Impinj Monza 4QT tag chip – alternate manufacturing location		
IPJ-W1513-E00	Impinj Monza 4D tag chip		
IPJ-W1513-F00	Impinj Monza 4D tag chip – alternate manufacturing location		
IPJ-W1535-E00*	Impinj Monza 4i tag chip*		

* Impinj Monza 4i tag chips have reached end-of-life (EOL) and are no longer available for sale.

8 NOTICES